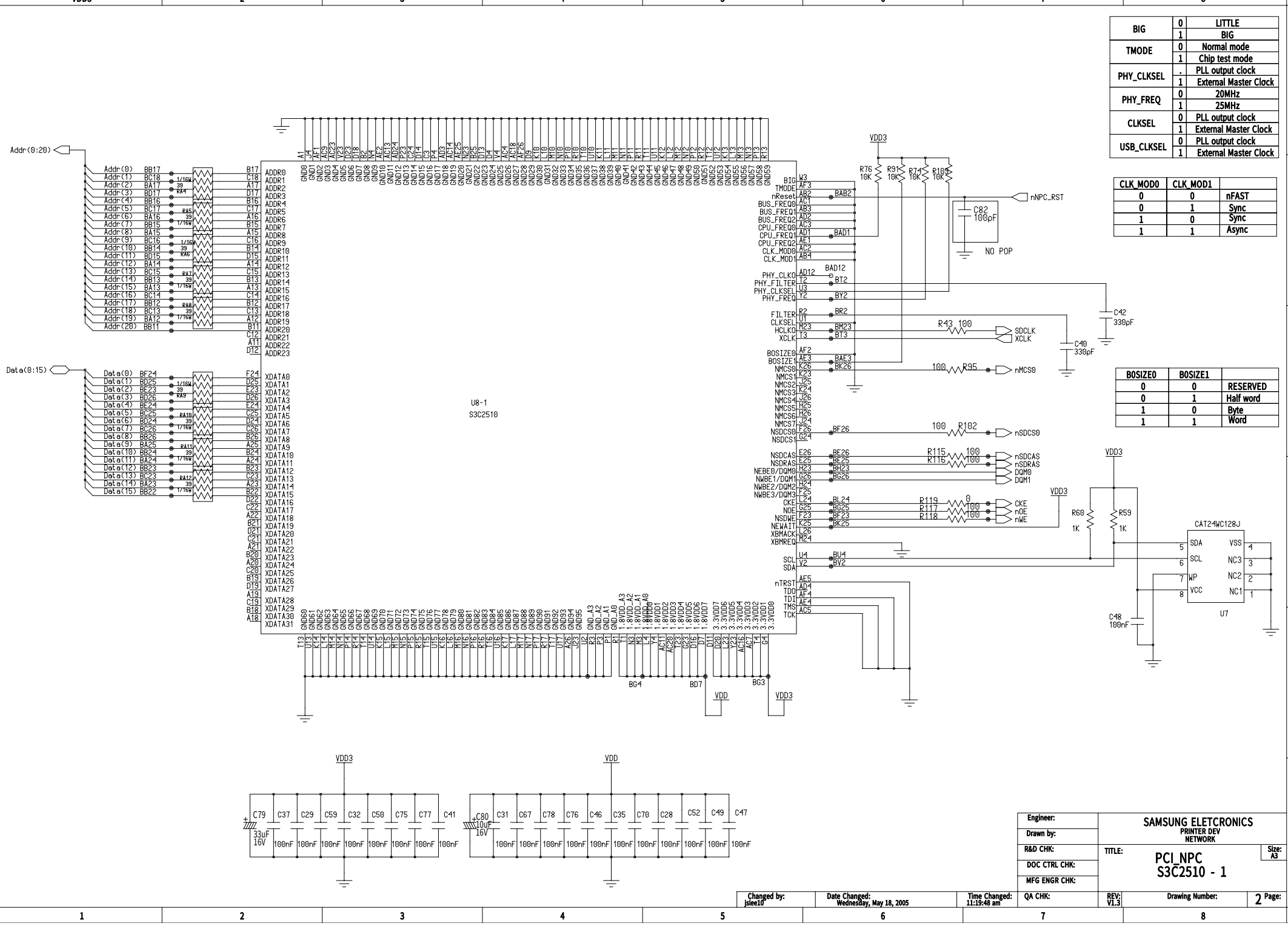
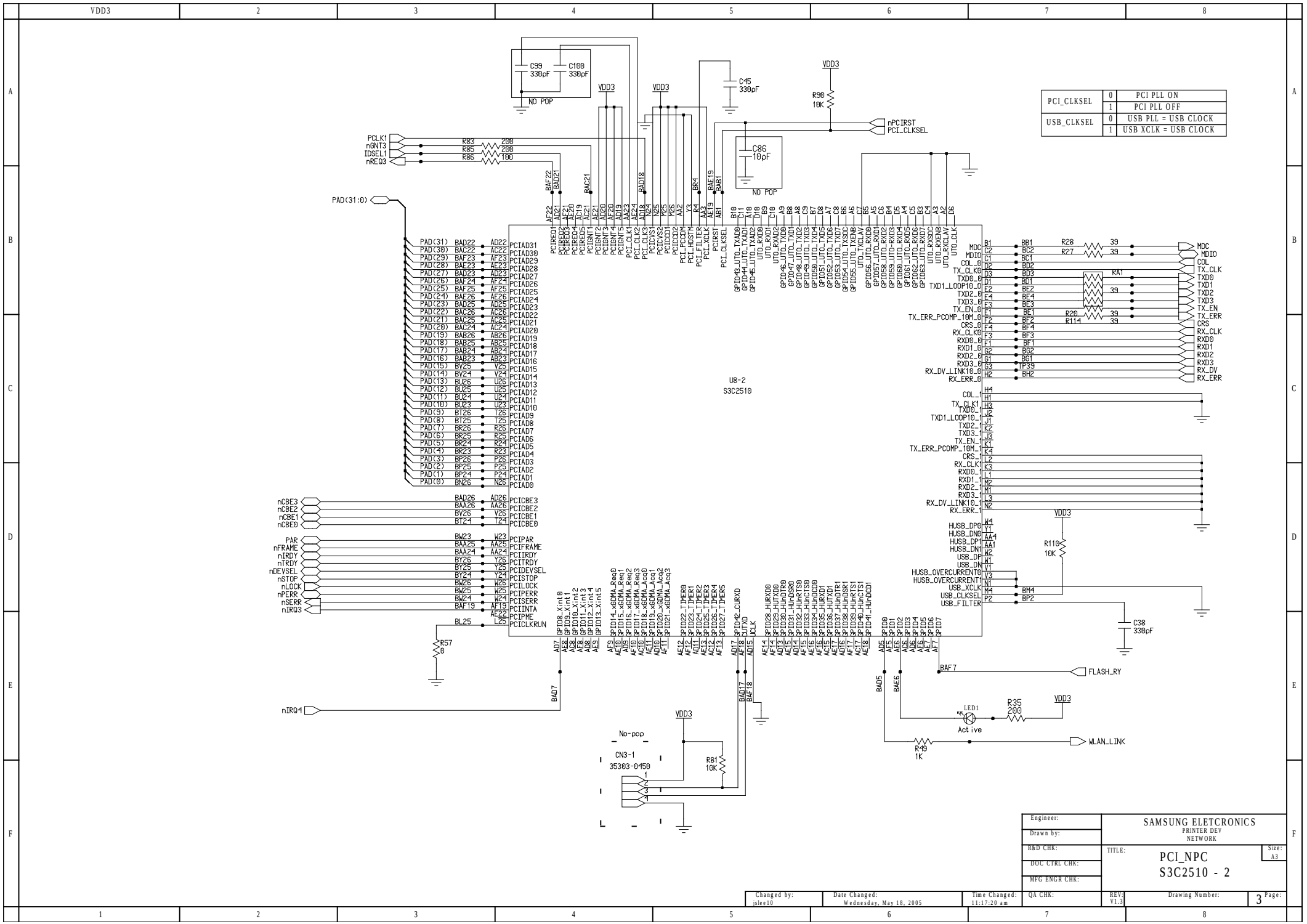

BIG 0 LITTLE
1 BIG
TMODE 0 Normal mode
1 Chip test mode
PHY_CLKSEL . PLL output clock
1 External Master Clock
PHY_FREQ 0 20MHz
1 25MHz
CLKSEL 0 PLL output clock
1 External Master Clock
USB_CLKSEL 0 PLL output clock
1 External Master Clock
CLK_MOD0 CLK_MOD1
0 0 nFAST
0 1 Sync
1 0 Sync
1 1 Async
BOSIZE0 BOSIZE1
0 0 RESERVED
0 1 Half word
1 0 Byte
1 1 Word
U8-1
S3C2510
Addr(0:20)
Data(0:15)
VDD3
VDD
nNPC_RST
NO POP
SDCLK
XCLK
nMCS0
nSDCS0
nSDCAS
nSDRAS
DQM0
DQM1
CKE
nOE
nWE
CAT24WC128J
SDA
SCL
WP
VCC
VSS
NC3
NC2
NC1
U7
Engineer:
Drawn by:
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
SAMSUNG ELETCRONICS
PRINTER DEV
NETWORK
TITLE:
PCI_NPC
S3C2510 - 1
Size: A3
Changed by: jslee10
Date Changed: Wednesday, May 18, 2005
Time Changed: 11:19:48 am
QA CHK:
REV: V1.3
Drawing Number:
2 Page:



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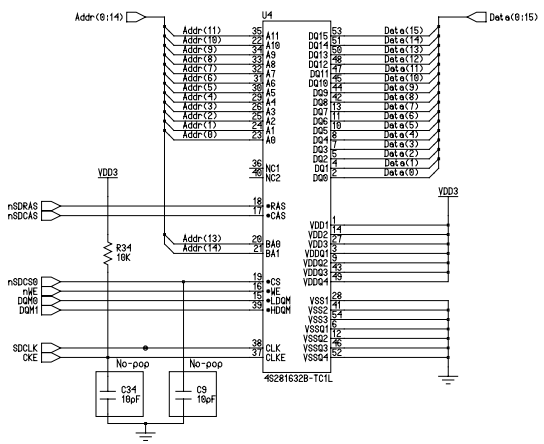
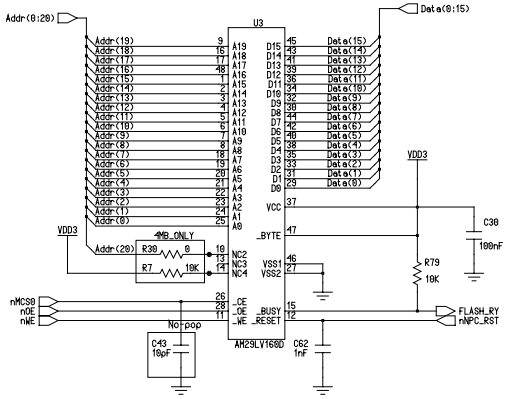
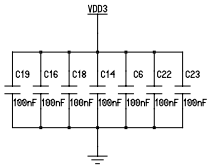
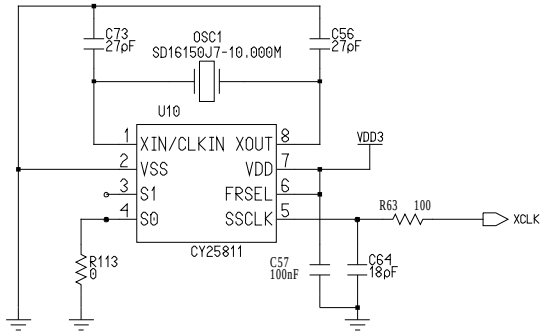


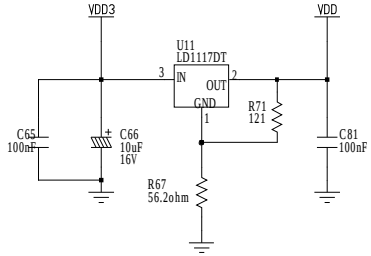




Changed by: jslee10	Date Changed: Wednesday, May 18, 2005	Time Changed: 11:17:55 am	QA CHK:

Engineer:	SAMSUNG ELETCRONICS PRINTER DEV NETWORK
Drawn by:	
R&D CHK:	TITLE: **PCI_NPC** Size: A3
DOC CTRL CHK:	FLASH ROM & SDRAM
MFG ENGR CHK:	
REV: V1.3	Drawing Number: Page: 4





Changed by: jslee10	Date Changed: Wednesday, May 18, 2005	Time Changed: 11:18:19 am	QA CHK:	REV: V1.3	Drawing Number:	Page: 5	

Engineer:	SAMSUN ELECTRONICS PRINTER DEV NETWORK	
Drawn by:		
R&D CHK:	TITLE: PCI_NPC POWER &CLOCK & RESET	Size: A3
DOC CTRL CHK:		
MFG ENGR CHK:		

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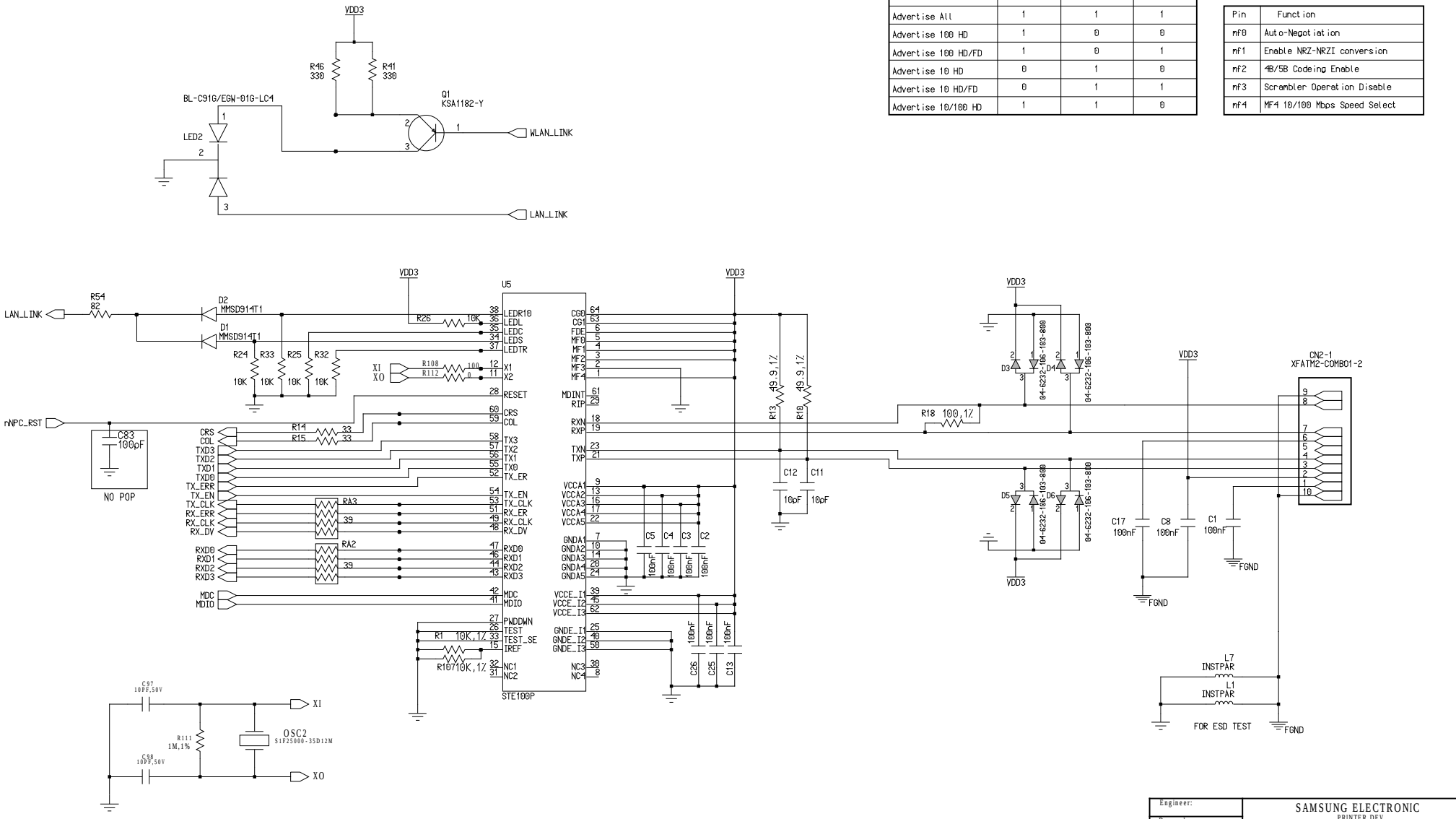
Operating Configurations/ Auto-Negotiation Enabled

Desired Configuration	Input Value		
	CFG0	CFG1	FDE
Advertise All	1	1	1
Advertise 100 HD	1	0	0
Advertise 100 HD/FD	1	0	1
Advertise 10 HD	0	1	0
Advertise 10 HD/FD	0	1	1
Advertise 10/100 HD	1	1	0

Multi-Function pins

Pin	Function
mf0	Auto-Negotiation
mf1	Enable NRZ-NRZI conversion
mf2	4B/5B Codeing Enable
mf3	Scrambler Operation Disable
mf4	MF4 10/100 Mbps Speed Select



Changed by: jslee10	Date Changed: Wednesday, May 18, 2005	Time Changed: 11:18:46 am	Engineer:	SAMSUNG ELECTRONIC PRINTER DEV NETWORK	
			Drawn by:		
			R&D CHK:	TITLE: PCI_NPC STE-100	Size: A3
			DOC CTRL CHK:		
			MFG ENGR CHK:		
			QA CHK:	REV: V1.3	Drawing Number: 6 Page:

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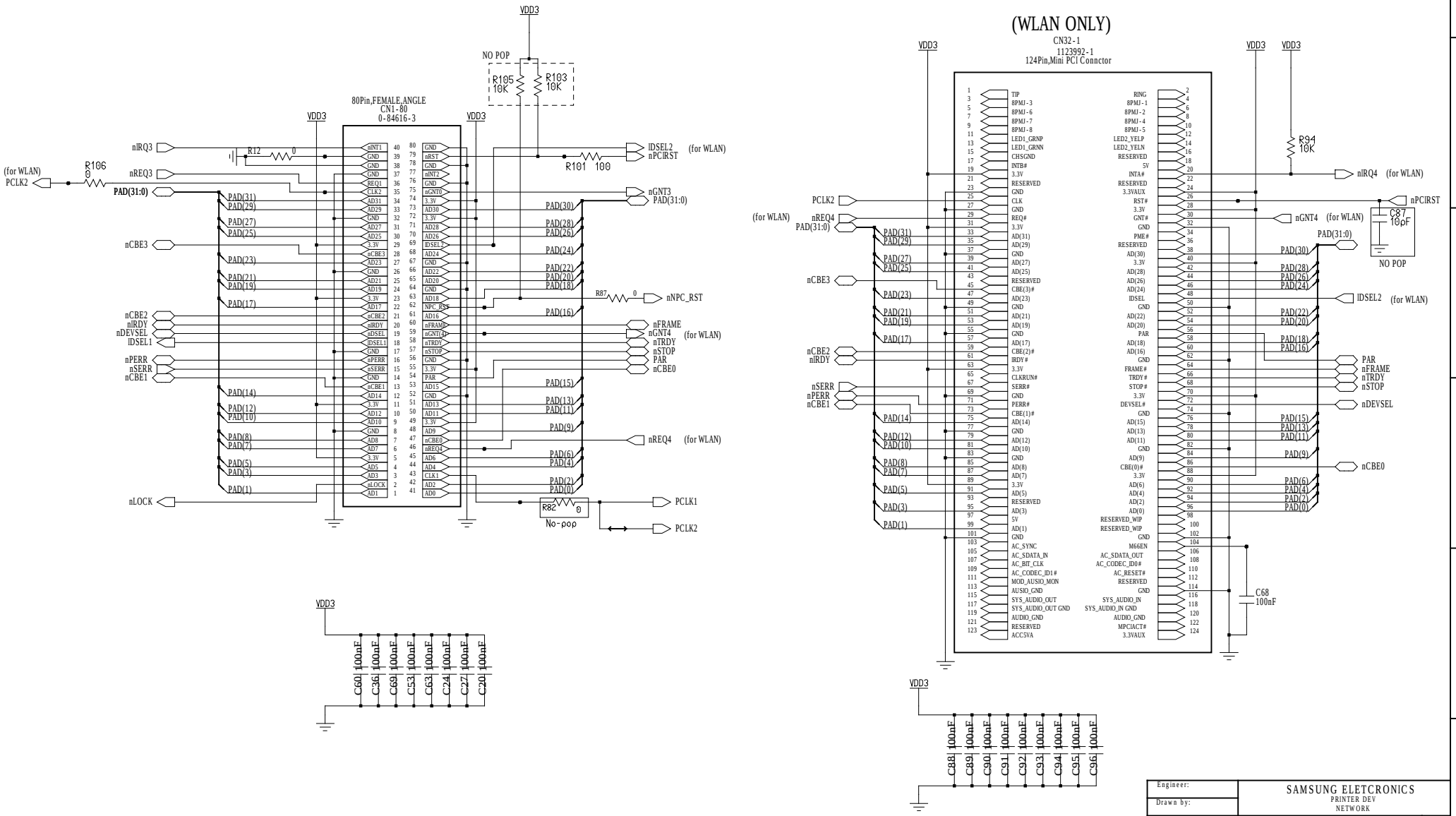

Engineer:	SAMSUNG ELETCRONICS PRINTER DEV NETWORK
Drawn by:	
R&D CHK:	TITLE: PCI_NPC PCI INTERFACE
DOC CTRL CHK:	Size: A3
MFG ENGR CHK:	

Changed by: jslee10	Date Changed: Wednesday, May 18, 2005	Time Changed: 11:19:11 am	QA CHK:	REV: V1.3	Drawing Number:	Page: 7

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