Repair Manual

Digital Laser MFP

SCX-5315F/SCX-5115

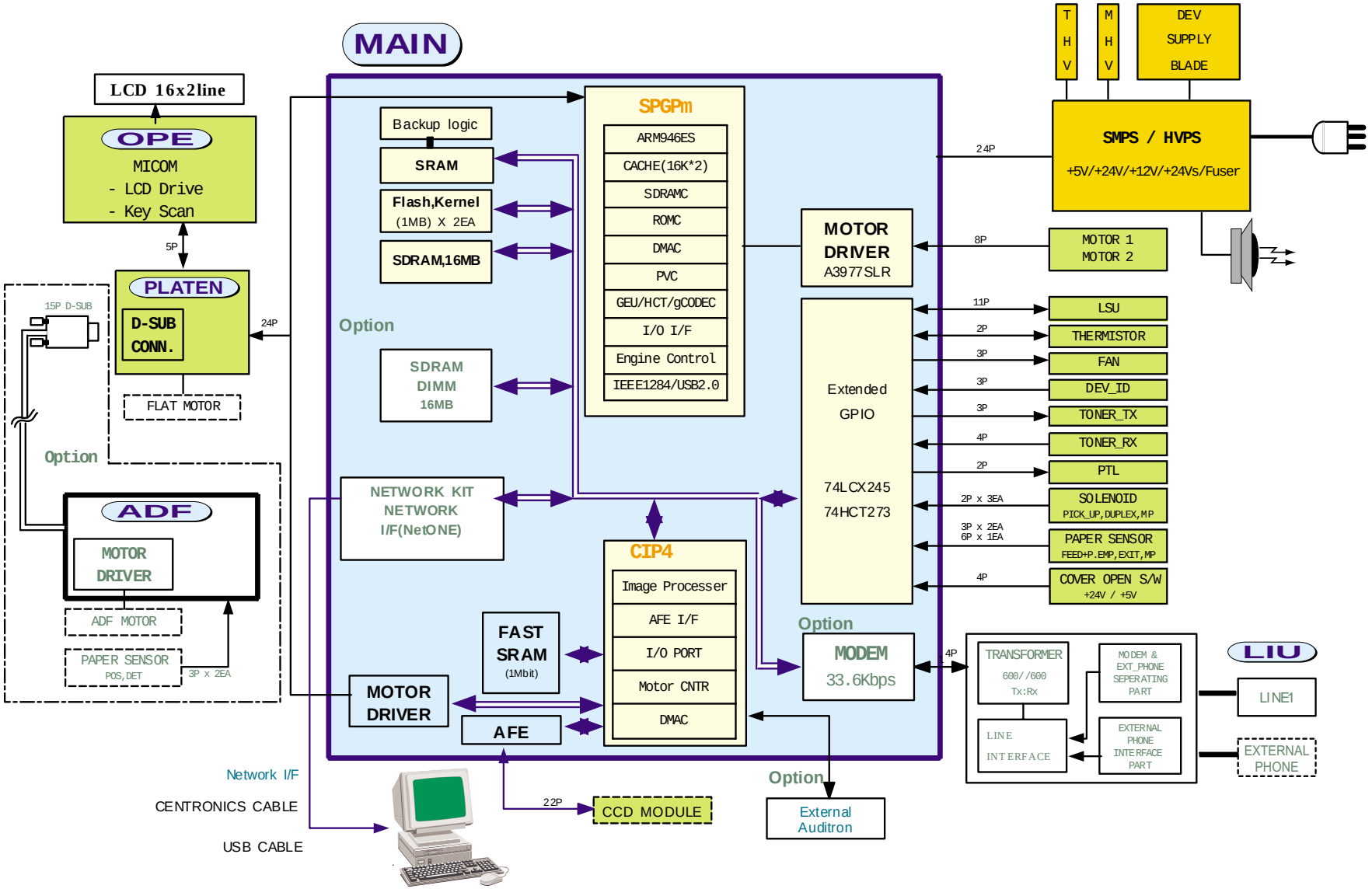
CONTENTS

SAMSUNG

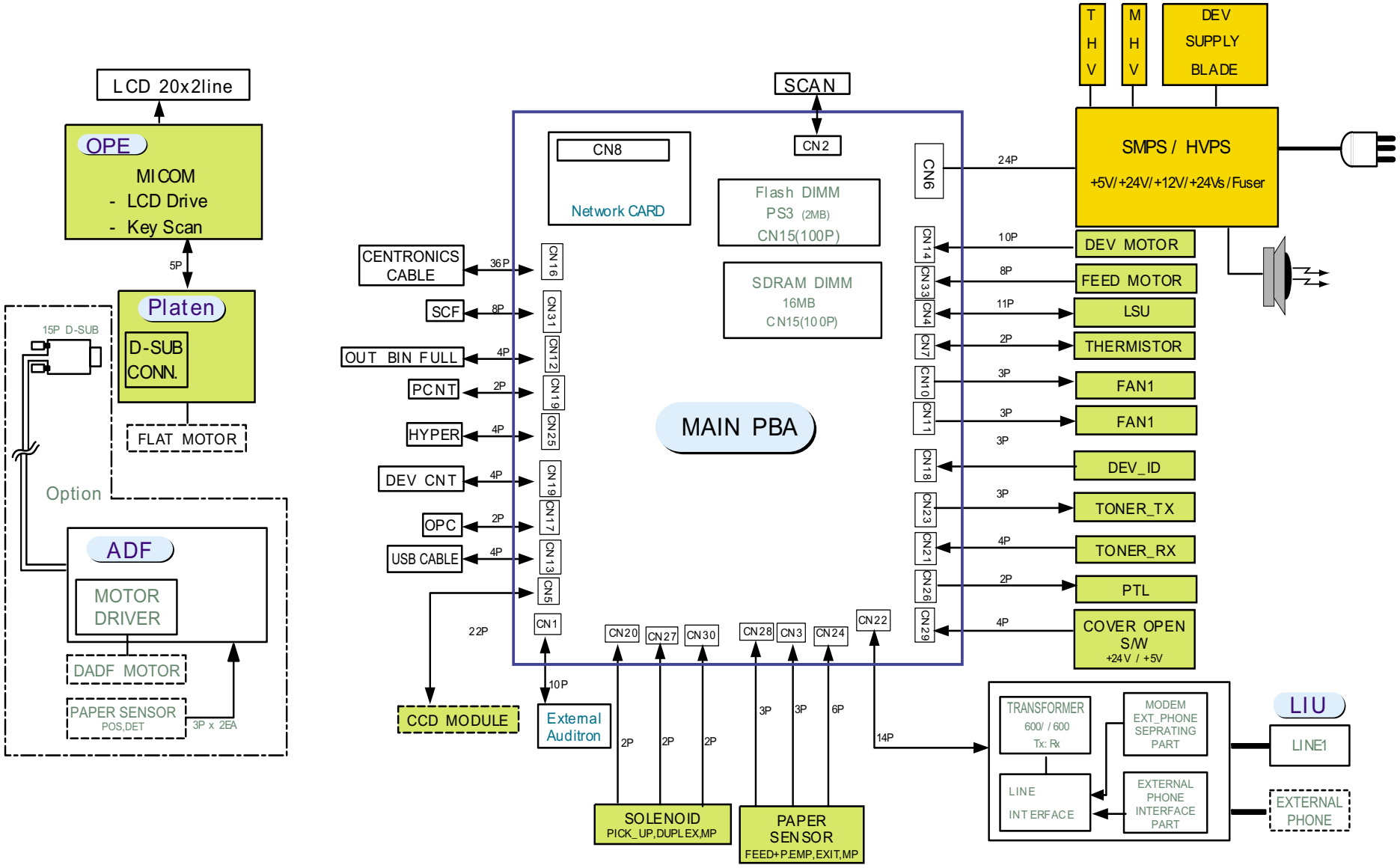
This manual is made and described centering around circuit diagram and circuit description needed in the repair center in the form of appendix.

Samsung Electronics Digital Printing
CS Group

1. Block Diagrams



2. Connection Diagrams

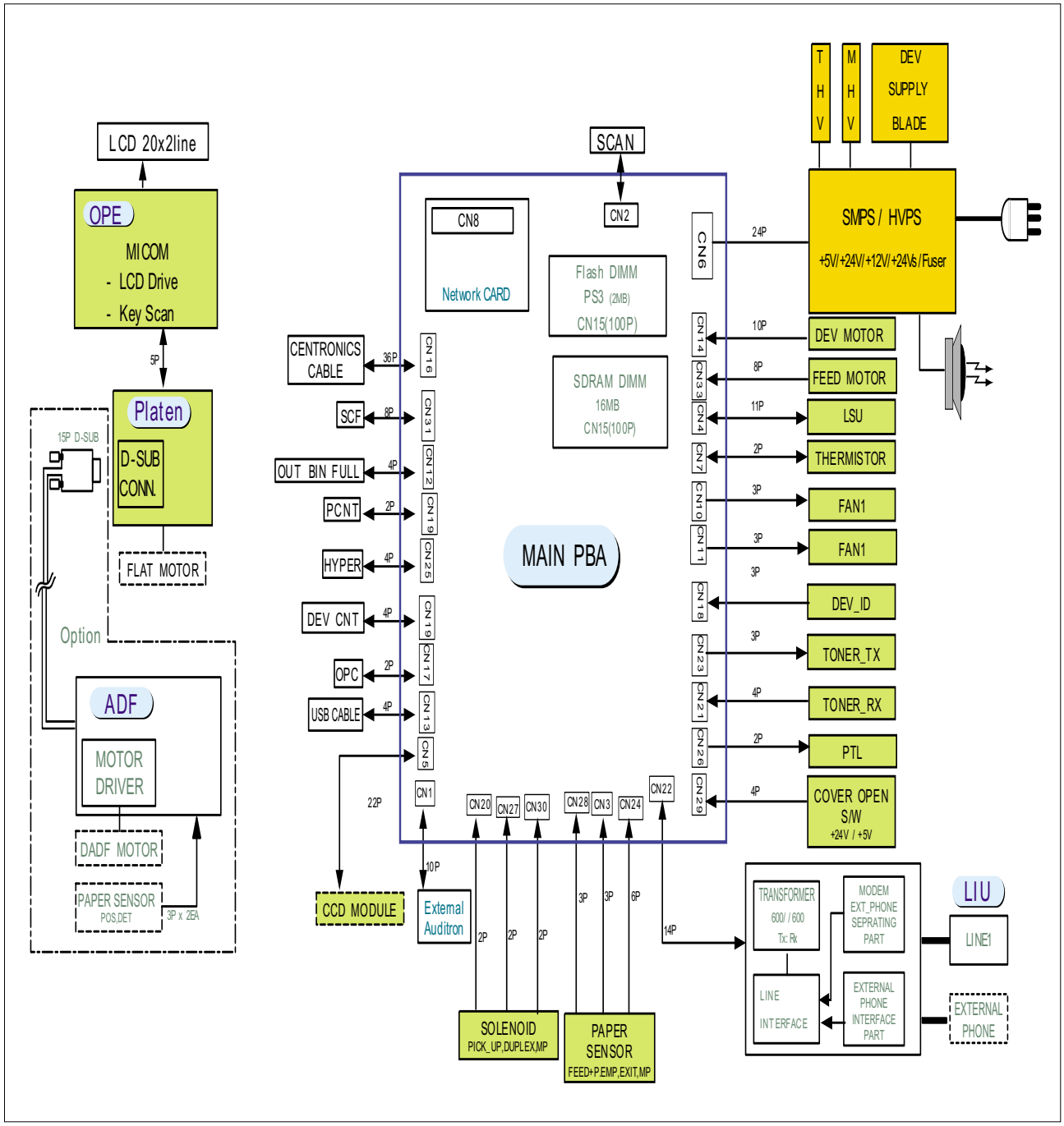


3. Circuit Description

3-1 Main PBA

3-1-1 Summary

The main circuit that consists of CPU, MFP controller (built-in 32bit RISC processor core: ARM946ES) including various I/O device drivers, system memory, scanner, printer, motor driver, PC I/F, and FAX transceiver controls the whole system. The entire structure of the main circuit is as follows :



<Block Diagram>

3-2 Circuit Operation

3-2-1 Clock

1) System Clock

Device	Oscillator
Frequency	12MHz

• ARM946ES RISC PROCESSOR: drives PLL internally uses 120MHz and external Bus uses 60 MHz.

2) Video Clock

Device	Oscillator
Frequency	57.0167MHz

• Fvd =((PAPER 1SCAN LINE sending time * SCAN effective late /1SCAN LINE DOT #)*4
=(600dpi*600dpi*58.208mm/s*216mm*4)/(25.4mm*25.4mm*76.1%)=28.697MHz
•PAPER 1SCAN LINE sending time=SCAN LINE interval/DOCUMENT SPEED (58.208mm/S)
•1SCAN LINE DOT #=MAZ SCAN distance(216mm)*DOT# per 1mm

3)USB Clock

Device	Oscillator
Frequency	48MHz

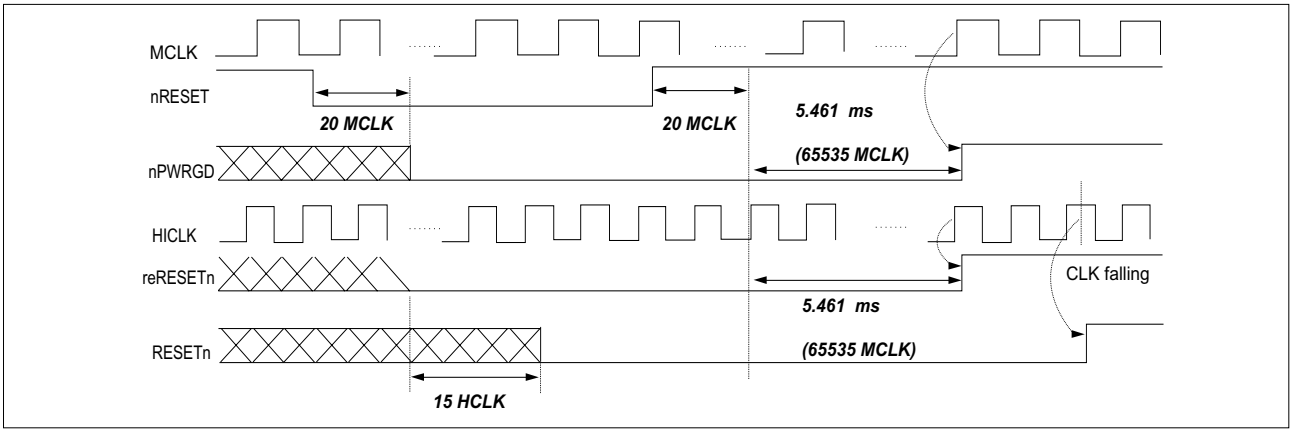
3-2-2 POWER ON/OFF RESET

1) Signal Operation

Input Signal +3.3V Power Line (VCC)
Output Signal ARM946ES nRESET and 29LU16ø
• POWER ON/OFF DETECT VCC RISING/FALLING 4.5°≠4.6V

RESET TIME (Td) 1.48~1.52ms
• Td=(Ct*V sensing)/I charge (...Ct=33µF, Is=100µA)

2) TIMING CHART



3-2-3 RISC MICROPROCESSOR

1) RISC MICROCESSOR PIN & INTERFACE(SPGPm)

Ball No	Pin No	Pin Name	I/O	Description	PAD
B1	1	SD15	I/O	SDRAM Bus Data[15]	BD8TARP_TC
C2	2	VSS_PLL1	-	VSS for Core PLL	-
D2	3	VDD_PLL1	-	VDD for Core PLL (1.8V)	-
D3	4	DATA0 / GPI1	I/O	ROM Bus Data[0] / GPI[1]	BD8TRP_FT
E4	5	MCLK	I	Core PLL Clock Input (12MHz)	TLCHT_TC
C1	6	DATA6 / GPI7	I/O	ROM Bus Data[6] / GPI[7]	BD8TRP_FT
D1	7	DATA1 / GPI2	I/O	ROM Bus Data[1] / GPI[2]	BD8TRP_FT
E3	8	DATA5 / GPI6	I/O	ROM Bus Data[5] / GPI[6]	BD8TRP_FT
E2	9	VDD_RING_OSC	-	VDD for Ring Oscillator (1.8V)	-
E1	10	DATA3 / GPI4	I/O	ROM Bus Data[3] / GPI[4]	BD8TRP_FT
F3	11	DATA9 / GPI10	I/O	ROM Bus Data[9] / GPI[10]	BD8TRP_FT
G4	12	GND	-	GROUND_RING	-
F2	13	DATA8 / GPI9	I/O	ROM Bus Data[8] / GPI[9]	BD8TRP_FT
F1	14	DATA7 / GPI8	I/O	ROM Bus Data[7] / GPI[8]	BD8TRP_FT
G3	15	DATA12 / GPI13	I/O	ROM Bus Data[12] / GPI[13]	BD8TRP_FT
G2	16	DATA11 / GPI12	I/O	ROM Bus Data[11] / GPI[12]	BD8TRP_FT
G1	17	DATA10 / GPI11	I/O	ROM Bus Data[10] / GPI[11]	BD8TRP_FT
H3	18	DATA4 / GPI5	I/O	ROM Bus Data[4] / GPI[5]	BD8TRP_FT
H2	19	DATA15 / GPI16	I/O	ROM Bus Data[15] / GPI[16]	BD8TRP_FT
H1	20	DATA14 / GPI15	I/O	ROM Bus Data[14] / GPI[15]	BD8TRP_FT
J4	21	VDD_CORE	-	VDD for CORE (1.8V)	-
J3	22	DATA19	I/O	ROM Bus Data[19]	BD8TRP_FT
J2	23	DATA18	I/O	ROM Bus Data[18]	BD8TRP_FT
J1	24	DATA17	I/O	ROM Bus Data[17]	BD8TRP_FT
K2	25	DATA16	I/O	ROM Bus Data[16]	BD8TRP_FT
K3	26	DATA22	I/O	ROM Bus Data[22]	BD8TRP_FT
K1	27	DATA13 / GPI14	I/O	ROM Bus Data[14] / GPI[14]	BD8TRP_FT
L1	28	DATA20	I/O	ROM Bus Data[20]	BD8TRP_FT
L2	29	DATA21	I/O	ROM Bus Data[21]	BD8TRP_FT
L3	30	DATA25	I/O	ROM Bus Data[25]	BD8TRP_FT
L4	31	DATA26	I/O	ROM Bus Data[26]	BD8TRP_FT
M1	32	DATA23	I/O	ROM Bus Data[23]	BD8TRP_FT
M2	33	DATA24	I/O	ROM Bus Data[24]	BD8TRP_FT
M3	34	DATA29	I/O	ROM Bus Data[29]	BD8TRP_FT
M4	35	DATA30	I/O	ROM Bus Data[30]	BD8TRP_FT
N1	36	DATA27	I/O	ROM Bus Data[27]	BD8TRP_FT
N2	37	DATA28	I/O	ROM Bus Data[28]	BD8TRP_FT
N3	38	VDD_ARM	-	VDD for ARM	-
P1	39	DATA31	I/O	ROM Bus Data[31]	BD8TRP_FT
P2	40	DATA2 / GPI3	I/O	ROM Bus Data[2] / GPI[3]	BD8TRP_FT
R1	41	VDD_CORE	-	VDD for CORE (1.8V)	-
P3	42	nROMCS2	O	ROM Bank2 Select_n	B4TR_TC

Ball No	Pin No	Pin Name	I/O	Description	PAD
R2	43	nRD	O	ROM Bus Read_n	B4TR_TC
T1	44	nROMCS0	O	ROM Bank0 Select_n	B4TR_TC
P4	45	nROMCS3 / nIOCS3 / GPO1	O	ROM Bank3 Select_n / IO Bank3 Select_n / GPO[1]	B4TR_TC
R3	46	nWR	O	ROM Bus Write_n	B4TR_TC
T2	47	nROMCS1	O	ROM Bank1 Select_n	B4TR_TC
U1	48	ADDR12	O	ROM Bus Addr[12]	B8TR_TC
T3	49	ADDR10	O	ROM Bus Addr[10]	B8TR_TC
U2	50	ADDR13	O	ROM Bus Addr[13]	B8TR_TC
V1	51	ADDR15	O	ROM Bus Addr[15]	B8TR_TC
T4	52	ADDR11	O	ROM Bus Addr[11]	B8TR_TC
U3	53	ADDR14	O	ROM Bus Addr[14]	B8TR_TC
V2	54	ADDR16	O	ROM Bus Addr[16]	B8TR_TC
W1	55	ADDR19	I/O	ROM Bus Addr[19]	BD8TRP_TC
V3	56	ADDR17	I/O	ROM Bus Addr[17]	BD8TRP_TC
W2	57	ADDR20	I/O	ROM Bus Addr[20]	BD8TRP_TC
Y1	58	nIOCS0	O	IO Bank0 Select_n	B4TR_TC
W3	59	ADDR21	I/O	ROM Bus Addr[21]	BD8TRP_TC
Y2	60	nIOCS1	O	IO Bank1 Select_n	B4TR_TC
W4	61	ADDR22	I/O	ROM Bus Addr[22]	BD8TRP_TC
V4	62	ADDR18	I/O	ROM Bus Addr[18]	BD8TRP_TC
U5	63	ADDR7	O	ROM Bus Addr[7]	B8TR_TC
Y3	64	VDD_CORE	O	VDD for CORE (1.8V)	-
Y4	65	nIOCS2 / nDACK0 / GPO2	O	IO Bank2 Select_n / DMA IO Bank0 ACK_n / GPO[2]	B4TR_TC
V5	66	ADDR1	O	ROM Bus Addr[1]	B8TR_TC
W5	67	ADDR8	O	ROM Bus Addr[8]	B8TR_TC
Y5	68	ADDR9	O	ROM Bus Addr[9]	B8TR_TC
V6	69	ADDR4	O	ROM Bus Addr[4]	B8TR_TC
U7	70	ADDR6	O	ROM Bus Addr[6]	B8TR_TC
W6	71	ADDR2	O	ROM Bus Addr[2]	B8TR_TC
Y6	72	ADDR3	O	ROM Bus Addr[3]	B8TR_TC
V7	73	ADDR5	O	ROM Bus Addr[5]	B8TR_TC
W7	74	VDD_ARM	-	VDD for ARM Hard Macro(1.8V)	-
Y7	75	VDD_CORE	-	VDD for CORE (1.8V)	-
V8	76	EINT0 / TnRST	I	Ext. Interrupt0 / TAP Controller Reset_n	SCHMITT_FT
W8	77	EINT1 / TCK	I	Ext. Interrupt1 / TAP Controller Clock	SCHMITT_FT
Y8	78	EINT2 / nRXD2 / TMS	I	Ext. Interrupt2 / UART RX DATA[2] / TAP Controller Mode Select	SCHMITT_FT
U9	79	EINT3 / nTXD2 / GPO9	I/O	Ext. Interrupt3 / UART TX Data[2] / GPO[9]	BD4STRP_FT
V9	80	nRxD0	I	UART RX Data[0]	SCHMITT_FT
W9	81	nRxD1 / GPI17 / TDI	I	UART RX Data[1] / GPI[17] / TAP Controller Data In	SCHMITT_FT
Y9	82	nTxD0	O	UART TX Data[0]	B4TR_TC
W10	83	TESTMODE	I	TESTMODE (Nomal : 0)	SCHMITT_TC

Ball No	Pin No	Pin Name	I/O	Description	PAD
V10	84	nTxD1 / GPO10 / TDO	O	UART Tx Data[1] / GPO[10] / Tap Controller Data Out	B4TR_TC
Y10	85	TESTSE	I	TESTSE (Normal : 0)	SCHMITT_TC
Y11	86	VDD_CORE	-	VDD for CORE (1.8V)	-
W11	87	RXERR / GPI25	I	MAC RX Error / GPI[25]	SCHMITT_TC
V11	88	GND	-	GROUND_RING	-
U11	89	RX_DV / GPI20	O	MAC RX Data Valid / GPI[20]	SCHMITT_TC
Y12	90	RXD0 / GPI21	O	MAC RX Data[0] / GPI[21]	SCHMITT_TC
W12	91	nLFPHB1 / nPRINT	O	Motor Out B_n / Print Start_n	B4TR_TC
V12	92	nLFPHB0 / nCMSG	O	Motor Out B / Command Message_n	B4TR_TC
U12	93	nLFPHA0 / CCLK	O	Motor Out A / Communication Clock	B4TR_TC
Y13	94	RXD1 / GPI22	I	MAC RX Data[1] / GPI[22]	SCHMITT_TC
W13	95	VDO	O	Video Data Out	B8TR_TC
V13	96	SPD / nDREQ3	I/O	DIMM Detect / DMA REQ[3]_n	BD4SRTP_TC
Y14	97	nWAIT1 / CRS	I	Wait_n / MAC Carrier Sensor	SCHMITT_TC
W14	98	COL / EINT4	I	MAC Collision Detect / Ext. Interrupt4	SCHMITT_TC
Y15	99	TX_EN	O	MAC TX Enable	B4TR_TC
V14	100	MDIO	I/O	MAC Management Data Inout	BD4STRUQP_TC
W15	101	TXD3 / GPO14	O	MAC TX Data[3] / GPO[14]	B4TR_TC
Y16	102	TXD2 / GPO13	O	MAC TX Data[2] / GPO[13]	B4TR_TC
U14	103	MDC / GPO15	O	MAC Management Data Clock / GPO[15]	B4TR_TC
V15	104	TXCLK / GPI18	I	MAC TX Clock(25MHz) / GPI[18]	SCHMITT_TC
W16	105	TXD1 / GPO12	O	MAC TX Data[1] / GPO[12]	B4TR_TC
Y17	106	PD4	I/O	Parallel Port Data[4]	BD4STRP_FT
V16	107	TXD0 / nIOCS3	O	MAC TX Data[0] / IO Bank3 Select_n	B4TR_TC
W17	108	RXD3 / GPI24	I	MAC RX Data[3] / GPI[24]	SCHMITT_TC
Y18	109	PD2	I/O	Parallel Port Data[2]	BD4STRP_FT
U16	110	PD6	I/O	Parallel Port Data[6]	BD4STRP_FT
V17	111	RXD2	I	MAC RX Data[2] / GPI[23]	SCHMITT_TC
W18	112	PWMOUT2	O	PWM Output[2]	B4TR_TC
Y19	113	VCLK	I	Video Reference Clock	TLCHT_TC
V18	114	RXCLK / GPI19	I	MAC RX Clock(25MHz) / GPI[19]	SCHMITT_TC
W19	115	PD1	I/O	Parallel Port Data[1]	BD4STRP_FT
Y20	116	nINIT	I	Parallel Port Initialization_n	SCHMITT_FT
W20	117	VSS_ADC	-	VSS for ADC	-
V19	118	ATEST_OUT	O	ADC Test Output	ANA_TC
U19	119	AIN2	I	ADC Channel2 Input	ANA_TC
U18	120	AIN1	I	ADC Channel1 Input	ANA_TC
T17	121	AIN0	I	ADC Channel0 Input	ANA_TC
V20	122	VDD_ADC	-	Analog power for ADC (3.3V)	-
U20	123	VDD_CORE	-	VDD for CORE (1.8V)	-
T18	124	GND	-	GROUND_RING	-
T19	125	VDD_CORE	-	VDD for CORE (1.8V)	-

Ball No	Pin No	Pin Name	I/O	Description	PAD
T20	126	VDD_CORE	-	VDD for CORE (1.8V)	-
R18	127	VBUS	I	USB Detect	SCHMITT_FT
P17	128	nLREADY / nEBSY	I	LSU Ready_n / Engine Busy_n	SCHMITT_FT
R19	129	nSELECTIN	I	Parallel Port Select Input_n	SCHMITT_FT
R20	130	LSUCLK / nCBSY / GPO11	O	LSU Clock / Command Busy_n / GPO[11]	B4TR_TC
P18	131	PD7	I/O	Parallel Port Data[7]	BD4STRP_FT
P19	132	PWMOUT1	O	PWM Output[1]	B4TR_TC
P20	133	PWMOUT0	O	PWM Output[0]	B4TR_TC
N18	134	nEMSG / nDACK3 / PWMOUT3	I/O	Engine Message_n / DMA ACK[3]_n / PWM Output[3]	BD4STRP_FT
N19	135	nFSYNC / nLFPHA1	I/O	Frame Sync_n / Motor Out A_n	BD4STRP_FT
N20	136	nHSYNC	I	Line Sync_n	SCHMITT_FT
M17	137	nSTROBE	I	Parallel Port Data Strobe_n	SCHMITT_FT
M18	138	PD5	I/O	Parallel Port Data[5]	BD4STRP_FT
M19	139	nWAIT0 / PDE	I/O	Wait_n / Parallel Port Data Enable	BD4STRP_TC
M20	140	nIOCS5 / nSCS4 / GPO3 / TONEOUT	O	DRAM Bank4 / IO Bank5 Select_n / GPO[3] / Tone Pulse Out	BD8TARP_TC
L19	141	PD3	I/O	Parallel Port Data[3]	BD4STRP_FT
L18	142	nFAULT	O	Parallel Port Fault_n	B4TR_TC
L20	143	nDREQ0 / GPI0 / ADDR23	I/O	DMA REQ[0]_n / GPI[0] / ADDR[23]	BD4STRP_TC
K20	144	nRESET	I	External Reset_n Input	SCHMITT_TC
K19	145	PERROR	O	Parallel Port Paper Error	B4TR_TC
K18	146	nAUTOFD	I	Parallel Port Auto Feed_n	SCHMITT_FT
K17	147	nDACK2 / DQM7 / GPO5	O	DMA ACK[2]_n / DQM[7] / GPO[5]	BD8TARP_TC
J20	148	nDREQ2 / DQM6 / GPO6	I/O	DMA REQ[2]_n / DQM[6] / GPO[6]	BD8TARP_TC
J19	149	nDREQ1 / DQM4 / GPO8	I/O	DMA REQ[1]_n / DQM[4] / GPO[8]	BD8TARP_TC
J18	150	VDD_CORE	-	VDD for CORE (1.8V)	-
J17	151	nSCS0	O	SDRAM Bank0 Select_n	BD8TARP_TC
H20	152	nSCS2	O	SDRAM Bank2 Select_n	BD8TARP_TC
H19	153	nCAS	O	SDRAM Column Address Select_n	BD8TARP_TC
H18	154	nSCS1	O	SDRAM Bank1 Select_n	BD8TARP_TC
G20	155	nIOCS4 / nSCS3 / GPO4	O	IO Bank4 / SDRAM Bank3 Select_n / GPO[4]	BD8TARP_TC
G19	156	BUSY	O	Parallel Port Busy	B4TR_TC
F20	157	PD0	I/O	Parallel Port Data[0]	BD4STRP_FT
G18	158	SLCT_OUT	O	Parallel Port Selection Out	B4TR_TC
F19	159	nACK	O	Parallel Port Acknowledge_n	B4TR_TC
E20	160	nDACK1 / DQM5 / GPO7	O	DMA ACK[1]_n / DQM[5] / GPO[7]	BD8TARP_TC
G17	161	nRSTOUT / CLKOUT / GPO0	O	Internal Reset_n Out / Internal System Clock Out / GPO[0]	B8TR_TC
F18	162	SA7	O	SDRAM Bus Addr[7]	BD8TARP_TC
E19	163	SA9	O	SDRAM Bus Addr[9]	BD8TARP_TC

Ball No	Pin No	Pin Name	I/O	Description	PAD
D20	164	VDD_USB	-	VDD for USB Hard Macro (1.8V)	-
E18	165	SA10	O	SDRAM Bus Addr[10]	BD8TARP_TC
D19	166	SA12	O	SDRAM Bus Addr[120	BD8TARP_TC
C20	167	BA0	O	SDRAM Bus Bank Select Addr[0]	BD8TARP_TC
E17	168	nRAS	O	SDRAM Row Address Select_n	BD8TARP_TC
D18	169	DQM2	O	SDRAM Bus DQM[2]	BD8TARP_TC
C19	170	DQM1	O	SDRAM Bus DQM[1]	BD8TARP_TC
B20	171	BA1	O	SDRAM Bus Bank Select Addr[1]	BD8TARP_TC
C18	172	DQM0	O	SDRAM Bus DQM[0]	BD8TARP_TC
B19	173	DQM3	O	SDRAM Bus DQM[3]	BD8TARP_TC
A20	174	RREF	I/O	USB PHY Register Reference	ANA_FT
A19	175	VSSL	-	VSS for Deserialisation Flip flops	-
B18	176	VDDL	-	VDD for Deserialisation Flip flops (1.8V)	-
B17	177	VSSB	-	VSS for buffers	-
C17	178	DMNS	I/O	USB2 DATA-	ANA_FT
D16	179	DPLS	I/O	USB2 DATA+	ANA_FT
A18	180	VDD3_USB	-	VDD for USB1.1 FS compliance (3.3V)	-
A17	181	VSSC	-	VSS for DLL and Xor tree	-
C16	182	VDDC	-	VDD for DLL and Xor tree (1.8V)	-
B16	183	VDDB	-	VDD for buffers (1.8V)	-
A16	184	VDD_USB	-	VDD for USB Hard Macro (1.8V)	-
C15	185	UCLK	I	USB PLL Input Clock (12MHz)	TLCHT_TC
D14	186	VSS_PLL2	-	VSS for USB PLL	-
B15	187	VDD_PLL2	-	VSS for USB PLL (1.8V)	-
A15	188	SA11	O	SDRAM Bus Addr[11]	BD8TARP_TC
C14	189	SA6	O	SDRAM Bus Addr[6]	BD8TARP_TC
B14	190	SA5	O	SDRAM Bus Addr[5]	BD8TARP_TC
A14	191	SA8	O	SDRAM Bus Addr[8]	BD8TARP_TC
C13	192	SA3	O	SDRAM Bus Addr[3]	BD8TARP_TC
B13	193	SA2	O	SDRAM Bus Addr[2]	BD8TARP_TC
A13	194	SA4	O	SDRAM Bus Addr[4]	BD8TARP_TC
D12	195	SA0	O	SDRAM Bus Addr[0]	BD8TARP_TC
C12	196	SA1	O	SDRAM Bus Addr[1]	BD8TARP_TC
B12	197	CKE	O	SDRAM Clock Enable	BD8TARP_TC
A12	198	nWE	O	SDRAM Write Enable_n	BD8TARP_TC
B11	199	SD30	I/O	SDRAM Bus Data[30]	BD8TARP_TC
C11	200	SD31	I/O	SDRAM Bus Data[31]	BD8TARP_TC
A11	201	SD29	I/O	SDRAM Bus Data[29]	BD8TARP_TC
A10	202	SD25	I/O	SDRAM Bus Data[25]	BD8TARP_TC
B10	203	SD26	I/O	SDRAM Bus Data[26]	BD8TARP_TC
C10	204	SD27	I/O	SDRAM Bus Data[27]	BD8TARP_TC
D10	205	SD28	I/O	SDRAM Bus Data[28]	BD8TARP_TC
A9	206	SD21	I/O	SDRAM Bus Data[21]	BD8TARP_TC
B9	207	SD22	I/O	SDRAM Bus Data[22]	BD8TARP_TC

Ball No	Pin No	Pin Name	I/O	Description	PAD
C9	208	SD23	I/O	SDRAM Bus Data[23]	BD8TARP_TC
D9	209	SD24	I/O	SDRAM Bus Data[24]	BD8TARP_TC
A8	210	SD18	I/O	SDRAM Bus Data[18]	BD8TARP_TC
B8	211	SDCLK0	O	SDRAM Clock Output0	BD8TARP_TC
C8	212	SD20	I/O	SDRAM Bus Data[20]	BD8TARP_TC
A7	213	SD14	I/O	SDRAM Bus Data[14]	BD8TARP_TC
B7	214	SD19	I/O	SDRAM Bus Data[19]	BD8TARP_TC
A6	215	SD11	I/O	SDRAM Bus Data[11]	BD8TARP_TC
C7	216	SD16	I/O	SDRAM Bus Data[16]	BD8TARP_TC
B6	217	SDCLK1	O	SDRAM Clock Output1	BD8TARP_TC
A5	218	SD12	I/O	SDRAM Bus Data[12]	BD8TARP_TC
D7	219	SD17	I/O	SDRAM Bus Data[17]	BD8TARP_TC
C6	220	SD13	I/O	SDRAM Bus Data[13]	BD8TARP_TC
B5	221	SD8	I/O	SDRAM Bus Data[8]	BD8TARP_TC
A4	222	SD5	I/O	SDRAM Bus Data[5]	BD8TARP_TC
C5	223	SD9	I/O	SDRAM Bus Data[9]	BD8TARP_TC
B4	224	SD6	I/O	SDRAM Bus Data[6]	BD8TARP_TC
A3	225	SD3	I/O	SDRAM Bus Data[3]	BD8TARP_TC
D5	226	SD10	I/O	SDRAM Bus Data[10]	BD8TARP_TC
C4	227	SD7	I/O	SDRAM Bus Data[7]	BD8TARP_TC
B3	228	SD4	I/O	SDRAM Bus Data[4]	BD8TARP_TC
B2	229	SD1	I/O	SDRAM Bus Data[1]	BD8TARP_TC
A2	230	SD0	I/O	SDRAM Bus Data[0]	BD8TARP_TC
C3	231	SD2	I/O	SDRAM Bus Data[2]	BD8TARP_TC

2) RISC MICROCESSOR PIN & INTERFACE(CIP4)

No	Pin Name	I/O	Description	Pad Type	Current drive
1	GND2	P	Vss Supply	vss2i	-
2	NTEST	I	Nand Tree Test Mode Selection	pticd	-
3	TM	I	Global Test Mode Selection	pticd	-
4	TEST1	I	Test Mode Selection 1	pticd	-
5	GND17	P	Vss Supply	vss3op	-
6	TEST2	I	Test Mode Selection 2	pticd	-
7	XDACK1	I	DMA Acknowledge Signal 1	ptis	-
8	XDREQ1	O	DMA Request Signal 1	phob4	4mA
9	VDD1	P	Vdd Supply	vdd2i	-
10	XDACK2	I	DMA Acknowledge Signal 2	ptis	-
11	XDREQ2	O	DMA Request Signal 2	phob4	4mA
12	XDACK3	I	DMA Acknowledge Signal 3	ptis	-
13	XDREQ3	O	DMA Request Signal 3	phob4	4mA
14	nRESET	I	Global Reset	ptis	-
15	CLK_OUT	O	PLL Clock Out	phob12	12mA
16	GND3	P	Vss Supply	vss2i	-
17	XP	I	Clock Oscillation Input	phsoscm26	10~40MHz
18	XPOUT	O	Clock Oscillation Output	phsoscm26	10~40MHz
19	GNDD16	P	Vss Supply	vss2t_abb	-
20	FILTER*	O	PLL Filter Pump Out	poar50_abb	-
21	GND1	P	Vss Supply	vbb_abb	-
22	VDDA9,VDDD9	P	Vdd Supply	vdd2t_abb	-
23	GND24,GND33	P	Vss Supply	vss3t_abb	-
24	RTC_XO	O	RTC Clock Oscillation Output	poar50_abb	-
25	RTC_XI	I	RTC Clock Oscillation Input	piar50_abb	-
26	VDD8,VDD18	P	Vdd Supply	vdd3t_abb	-
27	IRQ	O	Interrupt Request Signal	phob4	4mA
28	nCS	I	CIP4 Chip Select	ptis	-
29	GND4	P	Vss Supply	vss2i	-
30	nRD	I	CIP4 CPU Read Control	ptis	-
31	nWR	I	CIP4 CPU Write Control	ptis	-
32	BA1	I	Bank Address Bus [1]	ptis	-
33	BA0	I	Bank Address Bus [0]	ptis	-
34	GND19	P	Vss Supply	vss3op	-
35	A5	I	CPU Address Bus [5]	ptis	-
36	A4	I	CPU Address Bus [4]	ptis	-
37	A3	I	CPU Address Bus [3]	ptis	-
38	VDD2	P	Vdd Supply	vdd2i	-
39	A2	I	CPU Address Bus [2]	ptis	-
40	A1	I	CPU Address Bus [1]	ptis	-
41	A0	I	CPU Address Bus [0]	ptis	-
42	GND5	P	Vss Supply	vss2i	-
43	D31	B	CPU Data Bus [31]	phbst8	8mA

No	Pin Name	I/O	Description	Pad Type	Current drive
44	D30	B	CPU Data Bus [30]	phbst8	8mA
45	D29	B	CPU Data Bus [29]	phbst8	8mA
46	D28	B	CPU Data Bus [28]	phbst8	8mA
47	GND20	P	Vss Supply	vss3op	-
48	D27	B	CPU Data Bus [27]	phbst8	8mA
49	D26	B	CPU Data Bus [26]	phbst8	8mA
50	D25	B	CPU Data Bus [25]	phbst8	8mA
51	VDD11	P	Vdd Supply	vdd3op	-
52	D24	B	CPU Data Bus [24]	phbst8	8mA
53	D23	B	CPU Data Bus [23]	phbst8	8mA
54	D22	B	CPU Data Bus [22]	phbst8	8mA
55	D21	B	CPU Data Bus [21]	phbst8	8mA
56	GND6	P	Vss Supply	vss2i	-
57	D20	B	CPU Data Bus [20]	phbst8	8mA
58	D19	B	CPU Data Bus [19]	phbst8	8mA
59	D18	B	CPU Data Bus [18]	phbst8	8mA
60	GND21	P	Vss Supply	vss3op	-
61	D17	B	CPU Data Bus [17]	phbst8	8mA
62	D16	B	CPU Data Bus [16]	phbst8	8mA
63	D15	B	CPU Data Bus [15]	phbst8	8mA
64	D14	B	CPU Data Bus [14]	phbst8	8mA
65	VDD3	P	Vdd Supply	vdd2i	-
66	D13	B	CPU Data Bus [13]	phbst8	8mA
67	D12	B	CPU Data Bus [12]	phbst8	8mA
68	D11	B	CPU Data Bus [11]	phbst8	8mA
69	GND7	P	Vss Supply	vss2i	-
70	D10	B	CPU Data Bus [10]	phbst8	8mA
71	D9	B	CPU Data Bus [9]	phbst8	8mA
72	D8	B	CPU Data Bus [8]	phbst8	8mA
73	D7	B	CPU Data Bus [7]	phbst8	8mA
74	GND22	P	Vss Supply	vss3op	-
75	D6	B	CPU Data Bus [6]	phbst8	8mA
76	D5	B	CPU Data Bus [5]	phbst8	8mA
77	D4	B	CPU Data Bus [4]	phbst8	8mA
78	VDD12	P	Vdd Supply	vdd3op	-
79	D3	B	CPU Data Bus [3]	phbst8	8mA
80	D2	B	CPU Data Bus [2]	phbst8	8mA
81	D1	B	CPU Data Bus [1]	phbst8	8mA
82	D0	B	CPU Data Bus [0]	phbst8	8mA
83	GND8	P	Vss Supply	vss2i	-
84	TX_EN1	O	Motor Control Tx Enable 1	phob4	4mA
85	TX_EN2	O	Motor Control Tx Enable 2	phob4	4mA
86	TX_A	O	Motor Control Tx Channel A	phob4	4mA
87	TX_B	O	Motor Control Tx Channel B	phob4	4mA
88	GND23	P	Vss Supply	vss3op	-

No	Pin Name	I/O	Description	Pad Type	Current drive
89	nTX_A	O	Motor Control Tx Channel A	phob4	4mA
90	nTX_B	O	Motor Control Tx Channel A	phob4	4mA
91	MOTOR_POL	I	Motor Polarity	ptis	4mA
92	VDD4	P	Vdd Supply	vdd2i	-
93	PItg1	O	CIS/CCD PItg1 Signal	phob8	8mA
94	PI1	O	CIS/CCD PI1 Signal	phob8	8mA
95	PI2	O	CIS/CCD PI2 Signal	phob8	8mA
96	GND9	P	Vss Supply	vss2i	-
97	PIrs	O	CIS/CCD PIrs Signal	phob8	8mA
98	PIcp	O	CIS/CCD PIsh Signal	phob8	8mA
99	ADC_CLK	O	AFE ADC Clock	phob8	8mA
100	VDD13	P	Vdd Supply	vdd3op	-
101	CDS2_CLK	O	AFE CDS2 Clock	phob8	8mA
102	SCLK1	O	AFE SIO Sync. Clock	phob8	8mA
103	SLOAD1	O	AFE SIO Read/Write Control Signal	phob8	8mA
104	VDD10	P	Vdd Supply	vdd3op	-
105	SDO1	O	AFE SIO Serial Output 1	phob8	8mA
106	SDIO1	B	AFE SIO Serial Inout/Output 1	phbst8	8mA
107	SDIO2	B	AFE SIO Serial Inout/Output 2	phbst8	8mA
108	GND10	P	Vss Supply	vss2i	-
109	AFE_D9	I	A/D Converted Data Bus [9]	ptis	-
110	AFE_D8	I	A/D Converted Data Bus [8]	ptis	-
111	AFE_D7	I	A/D Converted Data Bus [7]	ptis	-
112	AFE_D6	I	A/D Converted Data Bus [6]	ptis	-
113	VDD5	P	Vdd Supply	vdd2i	-
114	AFE_D5	I	A/D Converted Data Bus [5]	ptis	-
115	AFE_D4	I	A/D Converted Data Bus [4]	ptis	-
116	AFE_D3	I	A/D Converted Data Bus [3]	ptis	-
117	GND25	P	Vss Supply	vss3op	-
118	AFE_D2	I	A/D Converted Data Bus [2]	ptis	-
119	AFE_D1	I	A/D Converted Data Bus [1]	ptis	-
120	AFE_D0	I	A/D Converted Data Bus [0]	ptis	-
121	GND11	P	Vss Supply	vss2i	-
122	SRAM_A15	O	SRAM Address Bus [15]	phob8	8mA
123	SRAM_A14	O	SRAM Address Bus [14]	phob8	8mA
124	SRAM_A13	O	SRAM Address Bus [13]	phob8	8mA
125	SRAM_A12	O	SRAM Address Bus [12]	phob8	8mA
126	VDD14	P	Vdd Supply	vdd3op	-
127	SRAM_A11	O	SRAM Address Bus [11]	phob8	8mA
128	SRAM_A10	O	SRAM Address Bus [10]	phob8	8mA
129	SRAM_A9	O	SRAM Address Bus [9]	phob8	8mA
130	GND26	P	Vss Supply	vss3op	-
131	SRAM_A8	O	SRAM Address Bus [9]	phob8	8mA
132	SRAM_A7	O	SRAM Address Bus [9]	phob8	8mA
133	SRAM_A6	O	SRAM Address Bus [9]	phob8	8mA

No	Pin Name	I/O	Description	Pad Type	Current drive
134	SRAM_A5	O	SRAM Address Bus [9]	phob8	8mA
135	GND12	P	Vss Supply	vss2i	-
136	SRAM_A4	O	SRAM Address Bus [9]	phob8	8mA
137	SRAM_A3	O	SRAM Address Bus [9]	phob8	8mA
138	SRAM_A2	O	SRAM Address Bus [9]	phob8	8mA
139	SRAM_A1	O	SRAM Address Bus [9]	phob8	8mA
140	VDD6	P	Vdd Supply	vdd2i	-
141	SRAM_A0	O	SRAM Address Bus [9]	phob8	8mA
142	SRAM_nWR	O	SRAM Write Enable Signal	phob8	8mA
143	SRAM_D15	B	SRAM Data Bus [15]	phbst8	8mA
144	SRAM_D14	B	SRAM Data Bus [14]	phbst8	8mA
145	GND27	P	Vss Supply	vss3op	-
146	SRAM_D13	B	SRAM Data Bus [13]	phbst8	8mA
147	SRAM_D12	B	SRAM Data Bus [12]	phbst8	8mA
148	SRAM_D11	B	SRAM Data Bus [11]	phbst8	8mA
149	GND13	P	Vss Supply	vss2i	-
150	SRAM_D10	B	SRAM Data Bus [10]	phbst8	8mA
151	SRAM_D9	B	SRAM Data Bus [9]	phbst8	8mA
152	SRAM_D8	B	SRAM Data Bus [8]	phbst8	8mA
153	SRAM_D7	B	SRAM Data Bus [7]	phbst8	8mA
154	VDD15	P	Vdd Supply	vdd3op	-
155	SRAM_D6	B	SRAM Data Bus [6]	phbst8	8mA
156	SRAM_D5	B	SRAM Data Bus [5]	phbst8	8mA
157	SRAM_D4	B	SRAM Data Bus [4]	phbst8	8mA
158	GND28	P	Vss Supply	vss3op	-
159	SRAM_D3	B	SRAM Data Bus [3]	phbst8	8mA
160	SRAM_D2	B	SRAM Data Bus [2]	phbst8	8mA
161	SRAM_D1	B	SRAM Data Bus [1]	phbst8	8mA
162	SRAM_D0	B	SRAM Data Bus [0]	phbst8	8mA
163	GND14	P	Vss Supply	vss2i	-
164	GPO7/PItg2	O	General Purpose Output [7]	phob8	8mA
165	GPO6/RLED	O	General Purpose Output [6]	phob8	8mA
166	GPO5/GLED	O	General Purpose Output [5]	phob8	8mA
167	GPO4/BLED	O	General Purpose Output [4]	phob8	8mA
168	VDD7	P	Vdd Supply	vdd2i	-
169	GPO3/PItg3	O	General Purpose Output [3]	phob8	8mA
170	GPO2/PIsh	O	General Purpose Output [2]	phob8	8mA
171	GPO1/ LEVEL_SHIFT	O	General Purpose Output [1]	phob8	8mA
172	GPO0	O	General Purpose Output [0]	phob8	8mA
173	GND29	P	Vss Supply	vss3op	8mA
174	GPIO2B/AFE_D11	B	General Purpose Input/Output 2 [11]	phbst8	8mA
175	GPIO2A/AFE_D10	B	General Purpose Input/Output 2 [10]	phbst8	-
176	GPIO29/AFE_D9	B	General Purpose Input/Output 2 [9]	phbst8	8mA
177	GND30	P	Vss Supply	vss3op	8mA
178	GPIO28/AFE_D8	B	General Purpose Input/Output 2 [8]	phbst8	8mA

No	Pin Name	I/O	Description	Pad Type	Current drive
179	GPIO27/AFE_D7	B	General Purpose Input/Output 2 [7]	phbst8	8mA
180	GPIO26/AFE_D6	B	General Purpose Input/Output 2 [6]	phbst8	-
181	GPIO25/AFE_D5	B	General Purpose Input/Output 2 [5]	phbst8	8mA
182	VDD16	P	Vdd Supply	vdd3op	8mA
183	GPIO24/AFE_D4	B	General Purpose Input/Output 2 [4]	phbst8	8mA
184	GPIO23/AFE_D3	B	General Purpose Input/Output 2 [3]	phbst8	8mA
185	GPIO22/AFE_D2	B	General Purpose Input/Output 2 [2]	phbst8	8mA
186	GND15	P	Vss Supply	vss2i	8mA
187	GPIO21/AFE_D1	B	General Purpose Input/Output 2 [1]	phbst8	8mA
188	GPIO20/AFE_D0	B	General Purpose Input/Output 2 [0]	phbst8	8mA
189	GPIO1F/ SRAM_D15	B	General Purpose Input/Output 1 [15]	phbst8	8mA
190	GPIO1E/ SRAM_D14	B	General Purpose Input/Output 1 [14]	phbst8	-
191	GND31	P	Vss Supply	vss3op	8mA
192	GPIO1D/ SRAM_D13	B	General Purpose Input/Output 1 [13]	phbst8	8mA
193	GPIO1C/ SRAM_D12	B	General Purpose Input/Output 1 [12]	phbst8	-
194	GPIO1B/ SRAM_D11	B	General Purpose Input/Output 1 [11]	phbst8	4mA
195	GPIO1A/ SRAM_D10	B	General Purpose Input/Output 1 [10]	phbst8	-
196	VDD17	P	Vdd Supply	vdd3op	
197	GPIO19/SRAM_D9	B	General Purpose Input/Output 1 [9]	phbst8	
198	GPIO18/SRAM_D8	B	General Purpose Input/Output 1 [8]	phbst8	
199	GPIO17/SRAM_D7	B	General Purpose Input/Output 1 [7]	phbst8	
200	GND32	P	Vss Supply	vss3op	
201	GPIO16/SRAM_D6	B	General Purpose Input/Output 1 [6]	phbst8	-
202	GPIO15/SRAM_D5	B	General Purpose Input/Output 1 [5	phbst8	-
203	GPIO14/SRAM_D4	B	General Purpose Input/Output 1 [4]	phbst8	-
204	GPIO13/SRAM_D3	B	General Purpose Input/Output 1 [3]	phbst8	-
205	GND18	P	Vss Supply	vss3op	-
206	GPIO12/SRAM_D2	B	General Purpose Input/Output 1 [2]	phbst8	-
207	GPIO11/SRAM_D1	B	General Purpose Input/Output 1 [1]	phbst8	-
208	GPIO10/SRAM_D0	B	General Purpose Input/Output 1 [0]	phbst8	-

3-2-4 PROGRAM ROM (FLASH MEMORY) CONTROL

1) DEVICE

TYPE No.	AM29LV160DB
CAPACITY	4 MBYTE (1MB * 16BITS * 2)

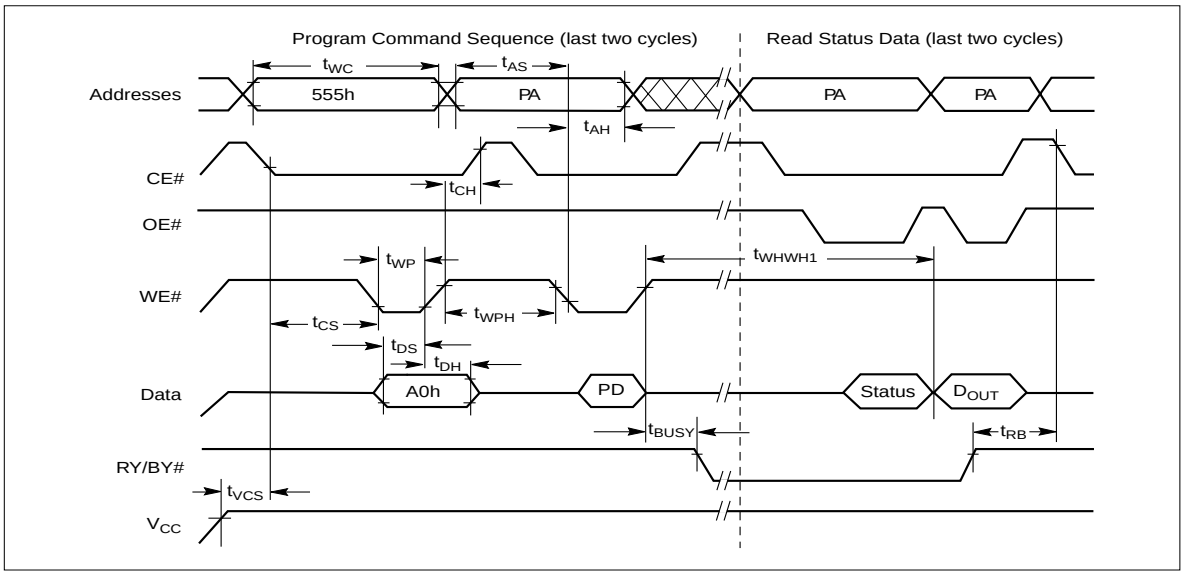
2) PROGRAMMING

BEFORE ASS'Y	EPROM PROGRAMMER or PROGRAMMING at the factory
AFTER ASS'Y	DOWNLOAD from PC

3) OPERATING PRINCIPLE

When the RCSO(ROM CHIP SELECT)signal is activated from the CPU after the POWER is ON, it activates RD SIGNAL and reads the DATA(HIGH/LOW) stored in the FLASH MEMORY to control the overall system. The FLASH MEMORY may also write. When turning the power on, press and hold the key(power switch) for 2 - 3 seconds, then the LED will scroll and the PROGRAM DOWNLOAD MODE will be activated. In this mode, you can download the program through the parallel port.

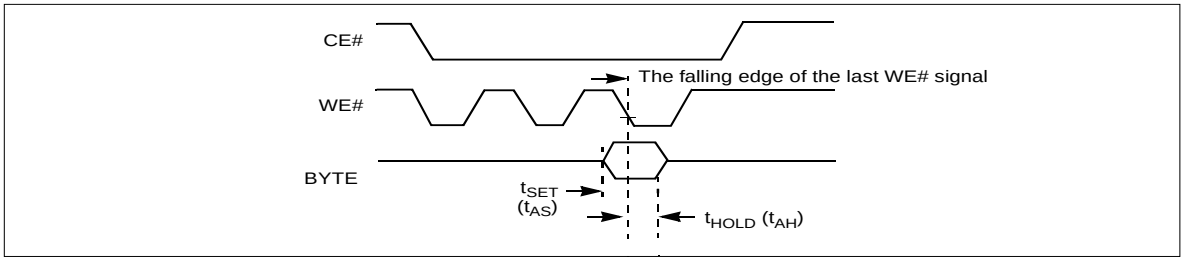
AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 16. BYTE# Timings for Write Operations

3-2-5 DRAM CONTROL

1) DEVICE

TYPE NO.	K4S
CAPACITY	16MBYTES (1M * 16BITS * 4Bank * 2)

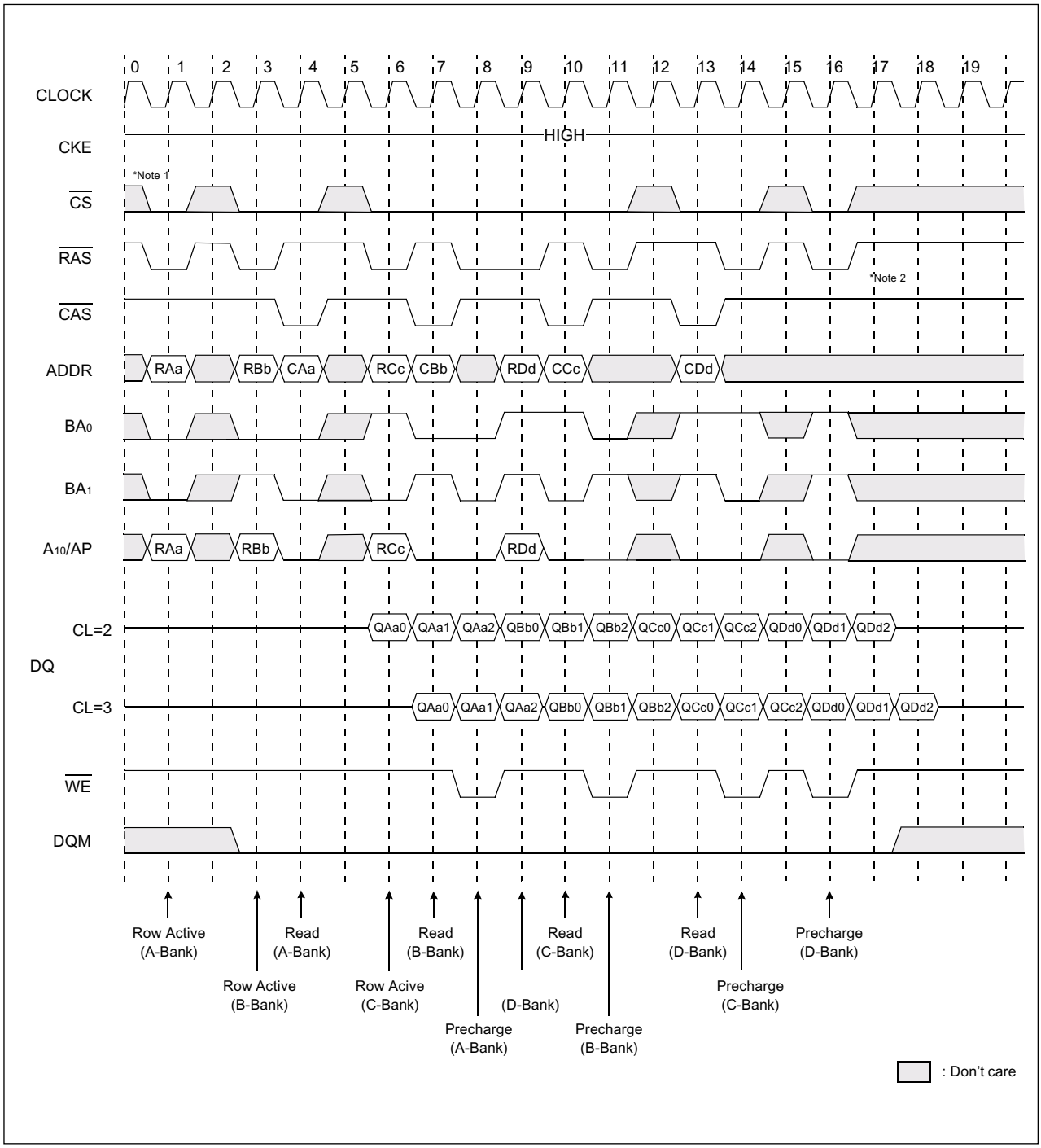
2) OPERATING PRINCIPLE

DRAM can either read or write. The data can be stored in the DRAM only when the power is on. It stores data white the CPU processes data. The address to read and write the data is specified by RAS SIGNAL and CAS SIGNAL. DRAMWE*SIGNAL is activated when writing data and DRAMOE*SIGNAL, when reading. You can expand up to 64MBYTE of DRAM in this system.

Start Address ~ End Address	Contents
0x00000000 ~ 0x00FFFFFF	ROM Bank0
0x01000000 ~ 0x01FFFFFF	ROM Bank1
0x02000000 ~ 0x02FFFFFF	ROM Bank2
0x03000000 ~ 0x03FFFFFF	ROM Bank3
0x04000000 ~ 0x0FFFFFFF	Unused
0x10000000 ~ 0x1FFFFFFF	Special Function Registers
0x20000000 ~ 0x20FFFFFF	I/O Bank0
0x21000000 ~ 0x21FFFFFF	I/O Bank1
0x22000000 ~ 0x22FFFFFF	I/O Bank2
0x23000000 ~ 0x23FFFFFF	I/O Bank3
0x24000000 ~ 0x24FFFFFF	I/O Bank4
0x25000000 ~ 0x25FFFFFF	I/O Bank5
0x26000000 ~ 0x26FFFFFF	DMA I/O Bank0
0x27000000 ~ 0x27FFFFFF	DMA I/O Bank1
0x28000000 ~ 0x28FFFFFF	DMA I/O Bank2
0x29800000 ~ 0x29FFFFFF	DMA I/O Bank3
0x2A000000 ~ 0x2FFFFFFF	Unused
0x30000000 ~ 0x30FFFFFF	RSH SRAM
0x31000000 ~ 0x31FFFFFF	HPVC SRAM
0x32000000 ~ 0x32FFFFFF	MOTOR SRAM
0x33000000 ~ 0x37FFFFFF	Unused
0x38000000 ~ 0x38FFFFFF	USB CSR & FIFO
0x39000000 ~ 0x390003FF	USB PLUG DETECT
0x38000500 ~ 0x3FFFFFFF	Unused
0x40000000 ~ 0x4FFFFFFF	SDRAM array0 (bank 0)
0x50000000 ~ 0x5FFFFFFF	SDRAM array1 (bank 1)
0x60000000 ~ 0x6FFFFFFF	SDRAM array2 (bank 2)
0x70000000 ~ 0x7FFFFFFF	SDRAM array3 (bank 3)
0x80000000 ~ 0xBFFFFFFF	SDRAM array0~4 (Mirror)
0xC0000000 ~ 0xC00007FF	MAC
0xC0000800 ~ 0xC0FFFFFF	Unused

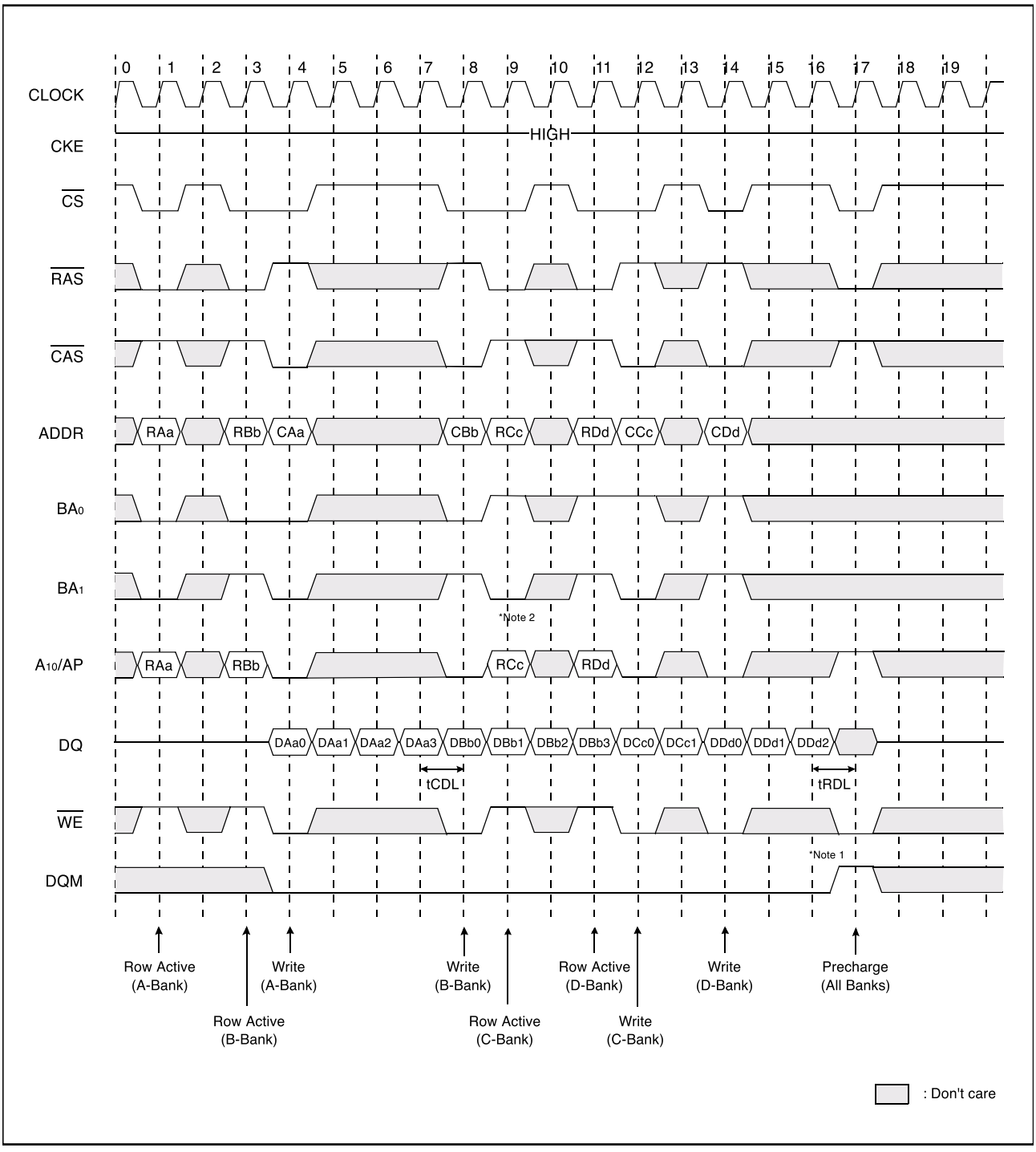
3-2-5-1 SDRAM read timing

Basically the Extended Data Out DRAM is similar to Fast Page Mode DRAM. For FPM, the data are valid only when the nCAS is active while reading the internal data, however, it has a latch that the data will be continuously outputted even after the nCAS is inactivated.
While configuring the software, you must set the timing register of SFR considering the clock speed and the DRAM spec.



* Note : 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are hih at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

3-2-5-2 SDRAM write timing



*Note : 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst wrige by Row precharge, both the write and the prechargebanks must be the same.

3-2-6 FS781 (FREQUENCY ATTENUATOR)

This system used FS741 for the main clock for EMI SUPPRESSION.
It spreads the source clock in a consistent bandwidth to disperse the energy gathered in order to attenuate the energy.
The capacitor value of the loop filter(PIN 4) is set depending on the source clock used or the spread bandwidth. Refer to FS781 Spec. for detail.

3-2-7 USB (Universal Serial Bus)

NS's USBN9602 is used as the interface IC and 48MHz clock is used.
When the data is received through the USB port, EIRQ1 SIGNAL is activated to send interrupt to CPU, then it directly sends the data to DRAM by IOCS4*&DRAMA(11) SIGNAL through DRAMD (24;31).

3-2-8 SRAM : 1MByte SRAM K6F1008U2C

It stores a variety of option data.

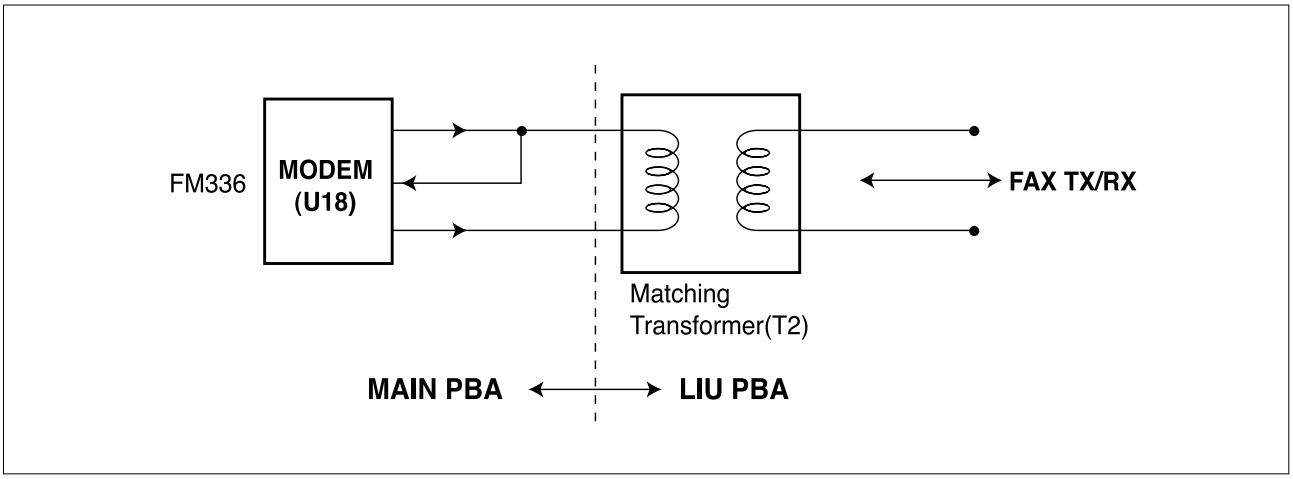
3-2-9 FAX Transceiver

3-2-9-1. GENERAL

This circuit processes transmission signals of modem and between LIU and modem.

3-2-9-2. modem (u44)

FM336 is a single ship fax modem. It has functions of DTMF detection and DTMF signal production as well as functioins of modem. TX A1, 2 is transmission output port and RX IN is received data input port. / POR signal controlled by MFP controller (U3:ARM946ES) can initialize modem (/M_RST) without turning off the system. D0-D7 are 8-bit data buses. RS0-RS4 signals to select the register in modem chips. /RS and /WR signals control READ and WRITE respectively. /IRQ is a signal for modem interrupt.
Transmission speed of FM336 is supported up to 33.6k.
The modem is connected to LINE through transformer directly.



< FAX TRANSCEIVER >

3-3 Scanner

3-3-1 SUMMARY

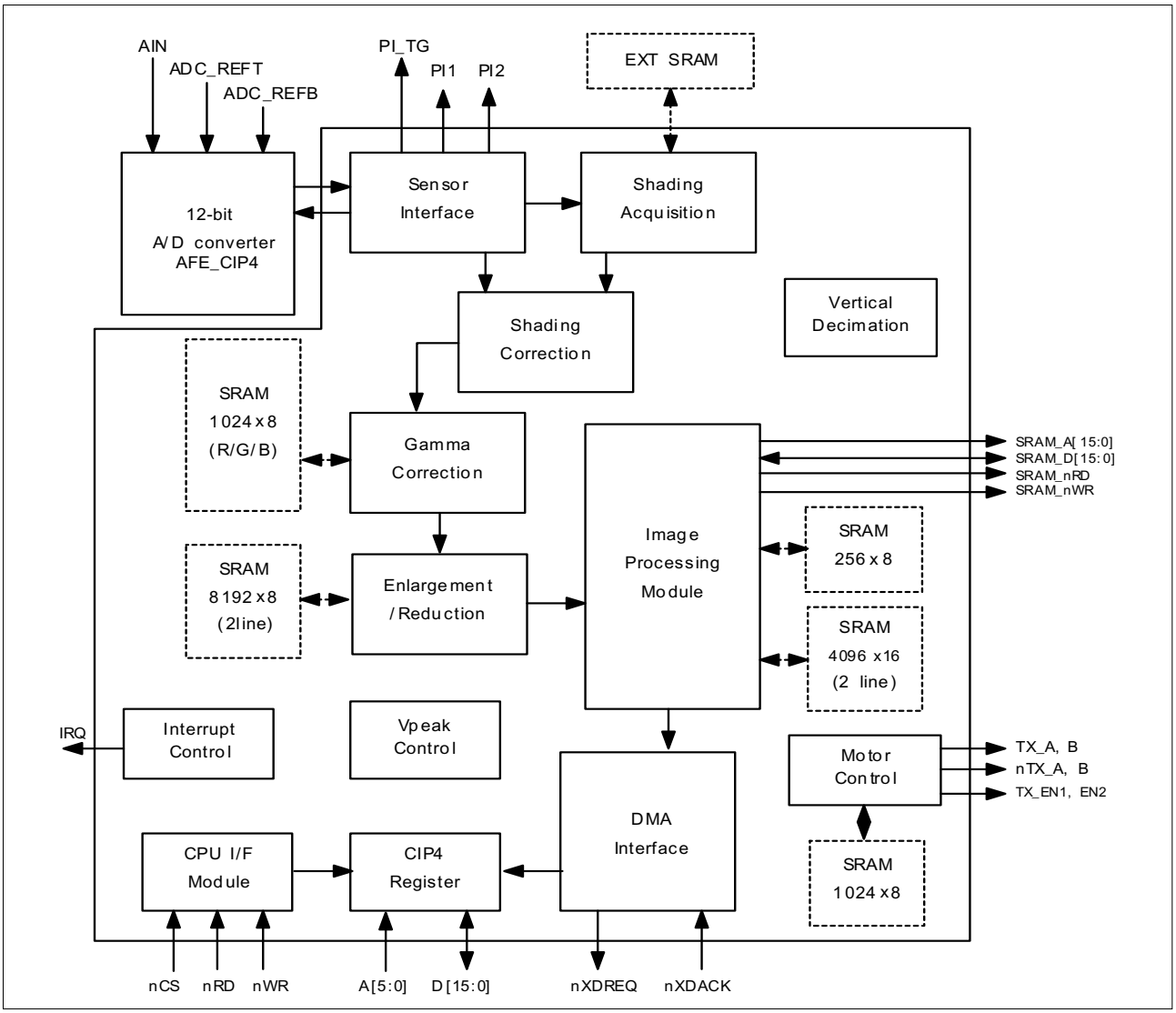
This flat-bed type device to read manuscripts has 600dpi CCD as an image sensor. There is one optical sensor for detecting CCD home position and Scan-end position. The home position is detected by a optical sensor which is attached to the CCD Module. The Scan-end position is calculated by numer of motor step.

CCD

Charge Coupled Device improves productivity and allows a compact design.

This machine uses a color CCD.

- Minimum Scan Line Time for One Color : 2.5mSec
- Light Source Power : +18V
- Maximum Pixel frequency : 10MHz
- Effective Sensor Element : 5340 X 3
- Clamp Level : 0.7~ 0.8V
- Bright Output : MIN 0.8V



<Block Diagram>

3-3-2 Key Features

Overview

(1) 0.5µm C-MOS process(TLM), 208-PIN QFP, STD85 library
(2) Frequency : Max PLL 80 MHz
(3) On-Chip oscillator
(4) Method : Raster scanning method
(5) Image Sauce : 300/400/600dpi CIS & CCD
(6) Scanning Mode
- color gray image: each 8 bits / RGB
- mono gray image: 8 bits / pixel
- binary image: 1 bit / pixel (for text/phoot/mixed mode)

(7) Maximum scanning width : A3, 600dpi (8K effective pixels)
(8) Ideal MSLT (A4, 600/300dpi)
- color gray image: 3x5Kx80nsec = 1.2msec (7/28 CPM)
- mono gray image: 1x5Kx80nsec = 0.4msec (21/84 CPM)
- binary image: 1x5Kx80nsec = 0.4msec (21/84 CPM)

(9) A/D conversion depth : 12bits

Pixel processing structure

- Minimum pixel processing time : 4 system clocks
- High speed pipelined processing method
(Shading correction, Gamma correction, Enlargement/Reducement, and Binarization)

Shading Correction

(1) White shading correction support for each R/G/B
(2) White shading data memory : 3x8Kx12bits = 288Kbits → 384Kbits (external)
(3) Black shading data memory : 3x8Kx12bits = 288Kbits → 384Kbits (external)

Gamma Correction

(1) Independent Gamma table for each RGB component
(2) Gamma table data memory : 3x1Kx8bits = 24Kbits (internal)

Binarization (mono)

(1) 256 Gray's halftone representation for Photo document : 3x5 EDF(Error DifFusion) method proposed by Stucki.
(2) LAT(Local Adaptive Thresholding) for Text document :
- use of 5x5 LOCAL WINDOW (TIP ALGORITHM)
- ABC(Automatic Background Control) :Tmin Automatic change

(3) Mixed mode processing for text/photo mixed document
(4) EDF data memory : 2x4Kx16bits = 128Kbits (internal)
(5) LAT data memory : 4x4Kx16bits = 256Kbits (external)

Scaling of input image

(1) Scaling factor
- Horizontal direction: 25 ~ 800% by 1% unit
- Vertical direction: 25 ~ 100% by 1% unit

(2) Scaling data memory : 2x8Kx8bits = 128Kbits (internal)

Intelligent scan motor controlloer

(1) Automatic acceleration/deceleration/uniform velocity
(2) Data memory : 256x16bits = 4Kbits (internal)

Auto-Run

Automatic CLK_LINE (line processing start control) and •'TG (line scan start control) signal generation|

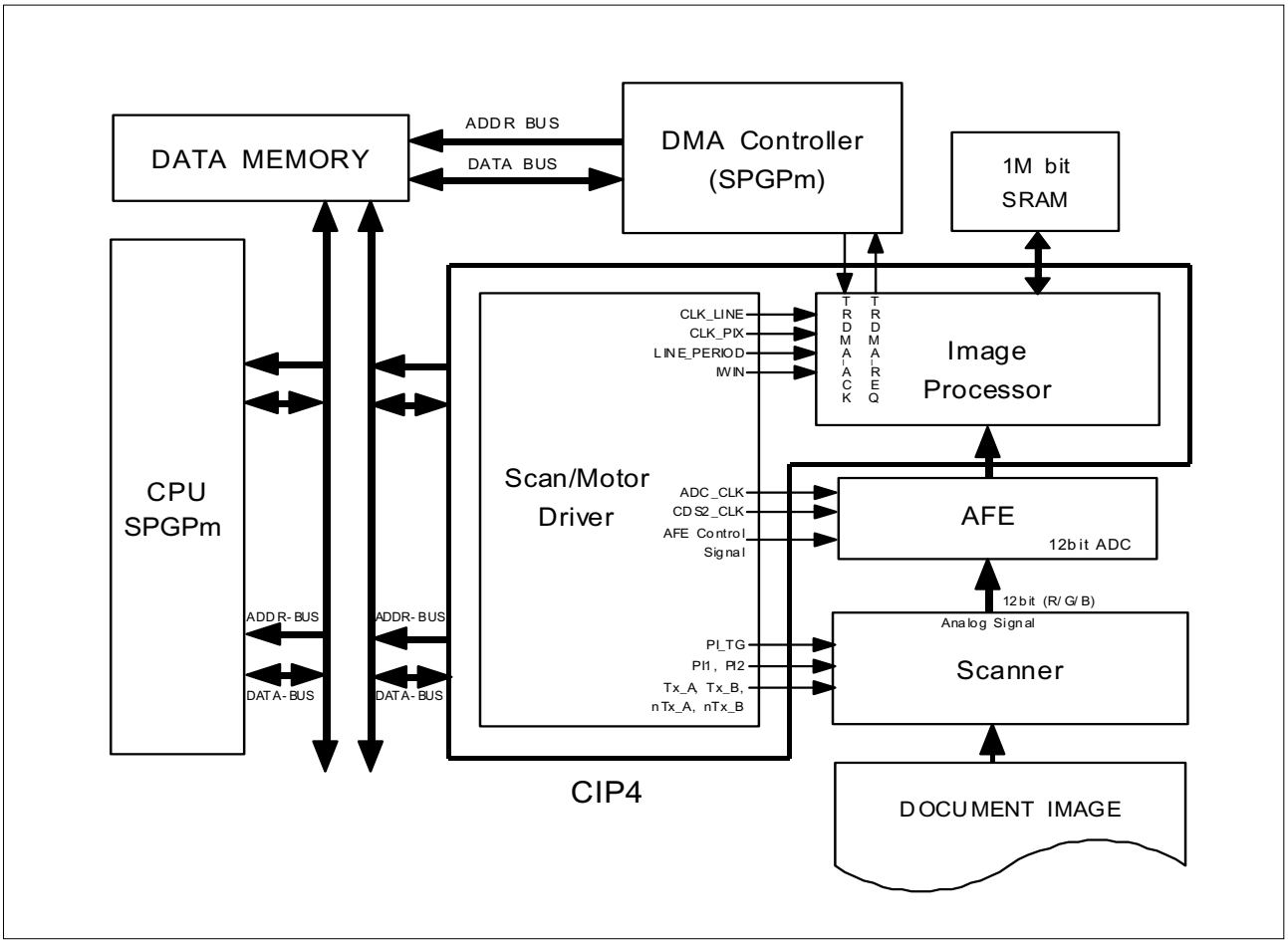
(1)Available resynchronization of øTG signal
(2) programmable øTG's period & CLK_LINE's occurrence number

Processed data output format in DTM(Data Transfer Module)

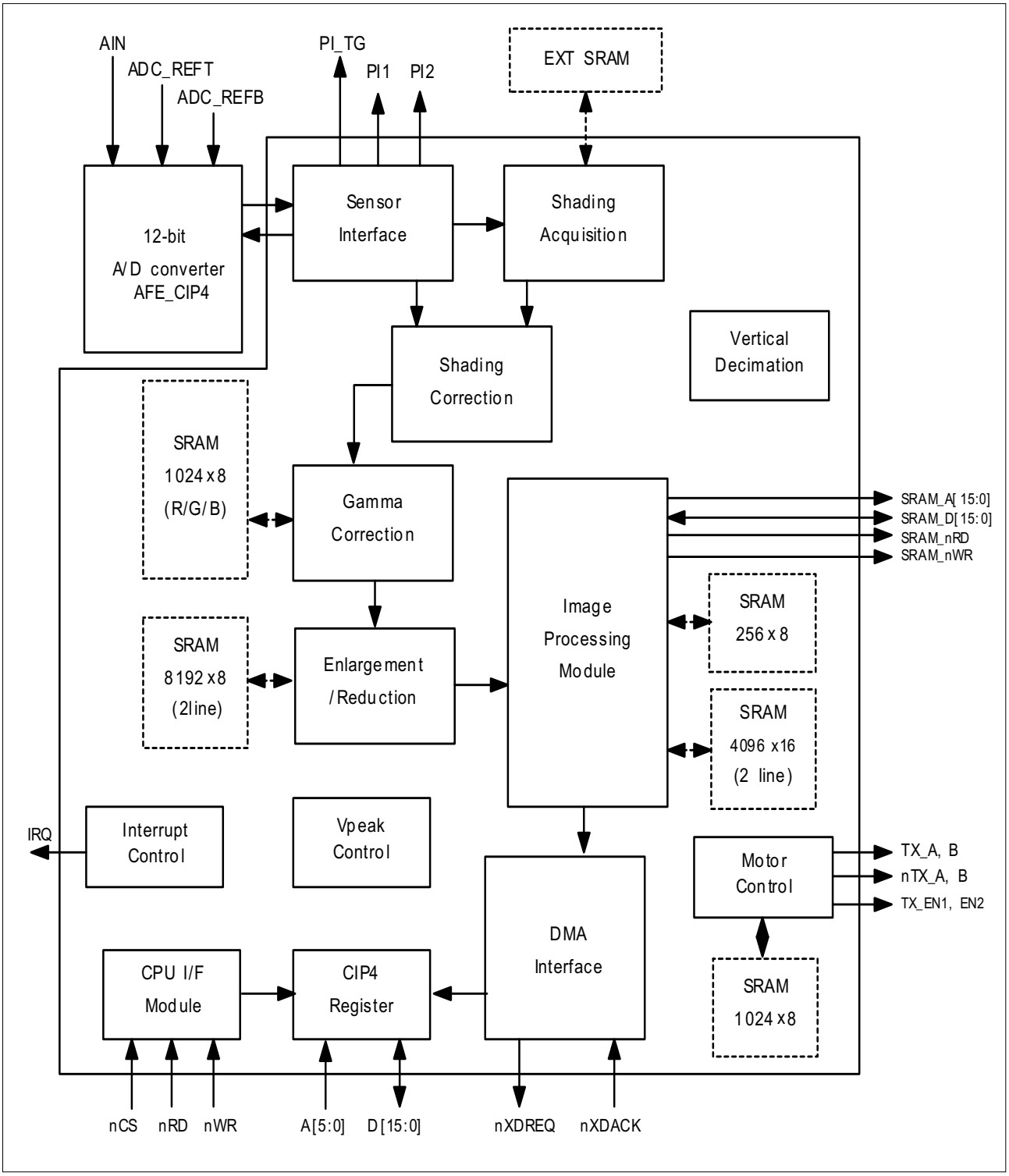
(1)DMA mode : Burst/On-demand mode
(2) CDIP I/F : LINE_SYNC, PIXEL_SYSNC, PIXEL_DATA[7:0]

36 General Purpose Input/Output : 8(GPO), 28(GPIO)

Black/White reversion, and Image Mirroring support



<External interfce with CIP4>



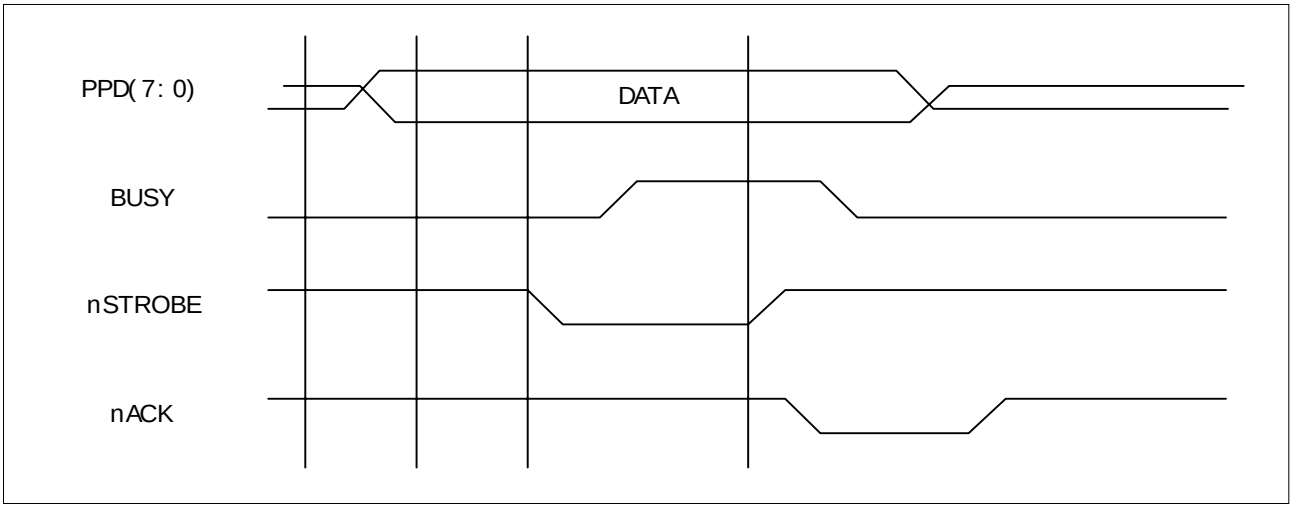
<Block diagram of CIP4>

3-4 HOST INTERFACE:

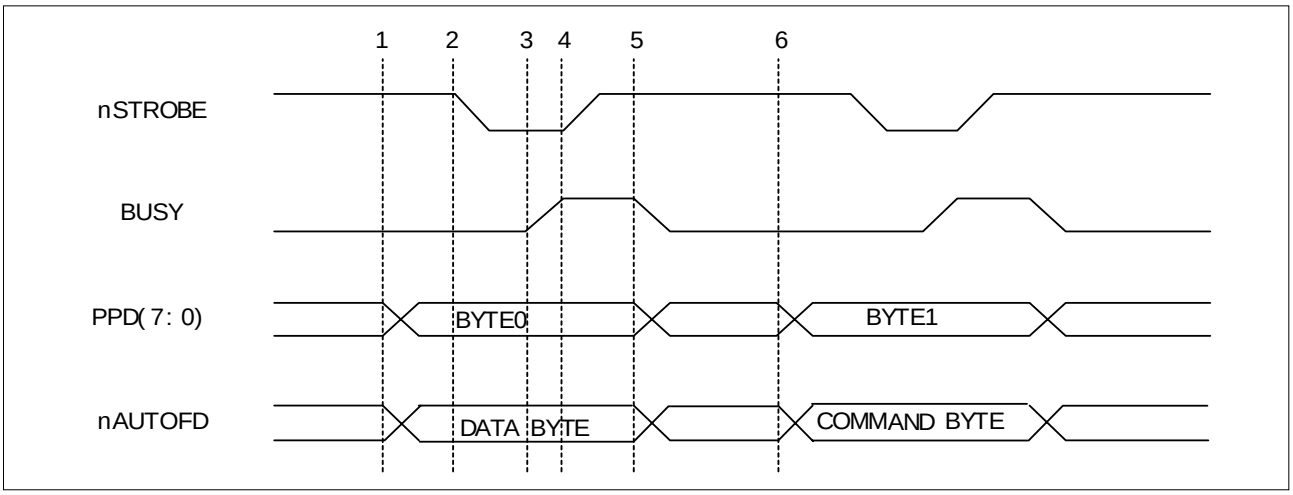
Referred to IEEE 1284 standard.

3-4-1. Host Interface

PARALLEL PORT INTERFACE PART ARM946ES has the Parallel Port Interface Part that enables Parallel Interface with PC. This part is connected to PC through Centronics connector. It generates major control signals that are used to actuate parallel communication. It is comprised of/ERROR, PE, BUSY, /ACK, SLCT, /INIT, /SLCTIN, /AUTOFD and /STB. This part and the PC data transmission method support the method specified in IEEE P1283 Parallel Port Standard (http://www.fapo.com/ieee1284.html). In other words, it supports both compatibility mode (basic print data transmitting method), the nibble mode (4bit data; supports data uploading to PC) and ECP (enhanced capabilities port: 8bits data - high speed two-way data transmission with PC). Compatibility mode is generally referred to as the Centronics mode and this is the protocol used by most PC to transmit data to the printer. ECP mode is an improved protocol for the communication between PC and peripherals such as printer and scanner, and it provides high speed two-way data communication. ECP mode provides two cycles in the two-way data transmission; data cycle and command cycle. The command cycle has two formats; Run-Length Count and Channel Addressing. RLE (Run-Length Count) has high compression rate (64x) and it allows real-time data compression that it is useful for the printer and scanner that need to transmit large raster image that has a series of same data. Channel Addressing was designed to address multiple devices with single structure. For example, like this system, when the fax/printer/scanner have one structure, the parallel port can be used for other purposes while the printer image is being processed.This system uses RLE for high speed data transmission. PC control signals and data send/receive tasks such as PC data printing, high speed uploading of scanned data to PC, upload/download of the fax data to send or receive and monitoring the system control signal and overall system from PC are all processed through this part.

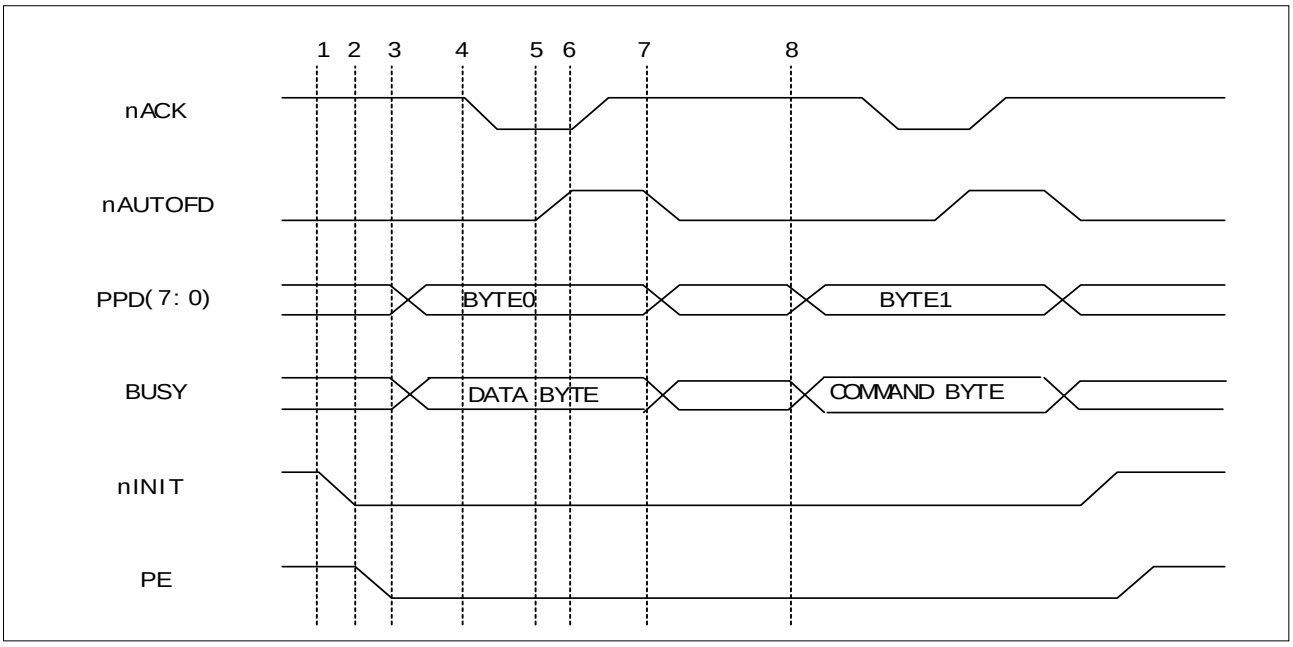


<Compatibility Hardware Handshaking Timing>



<ECP Hardware Handshaking Timing (forward) >

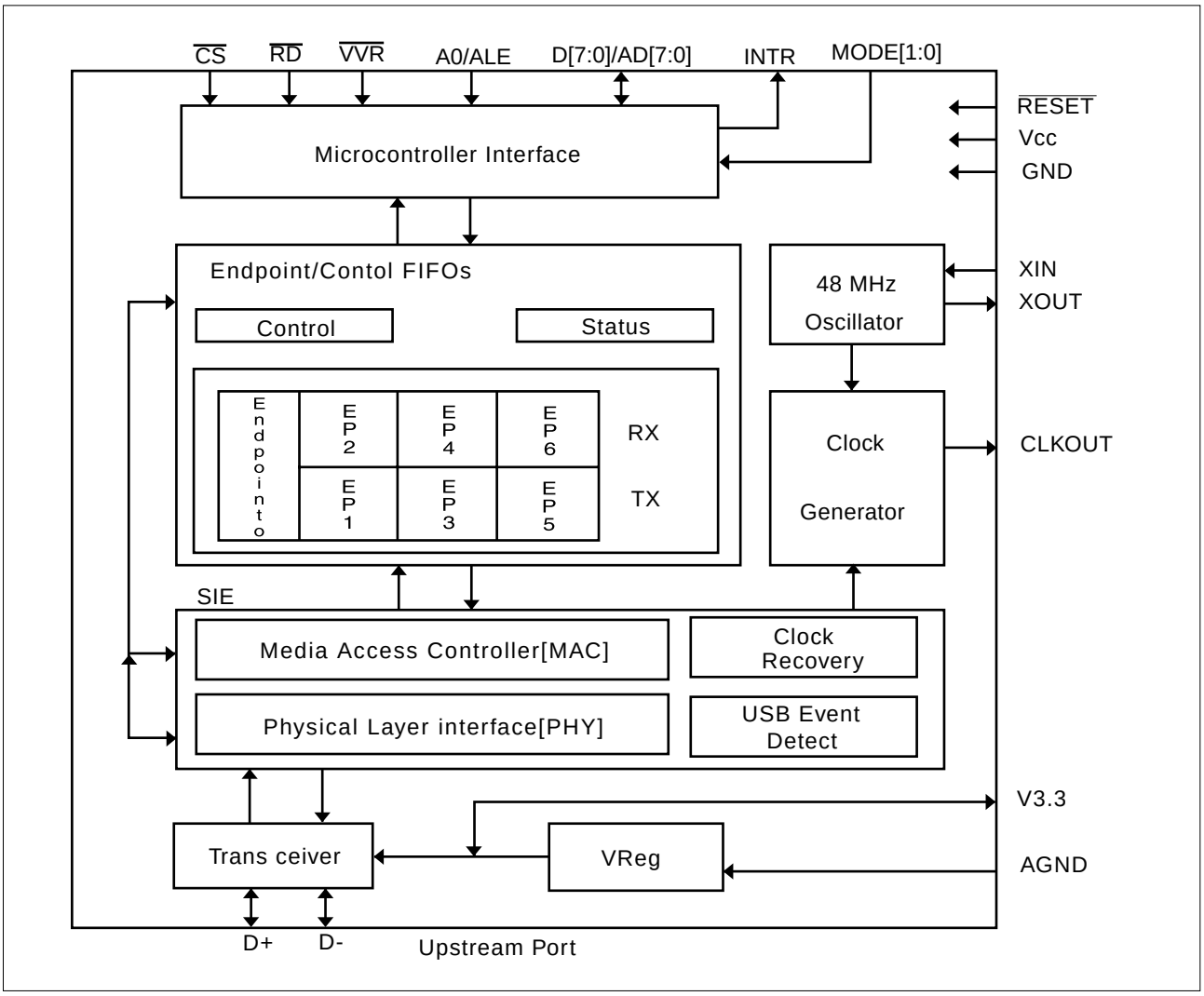
1. The host places data on the data lines and indicates a data cycle by setting nAUTOFD
2. Host asserts nSTROBE low to indicate valid data
3. Peripheral acknowledhes host by setting BUSY high
4. Host sets nSTROBE high. This is the edge that should be used to clock the data into the Peripheral
5. Peripheral sets BUSY low to indicate that it is ready for the next byte
6. The cycle repeats, but this time it is a command cycle because nAUTOFD is low



<ECP Hardware Handshaking Timing (forward)

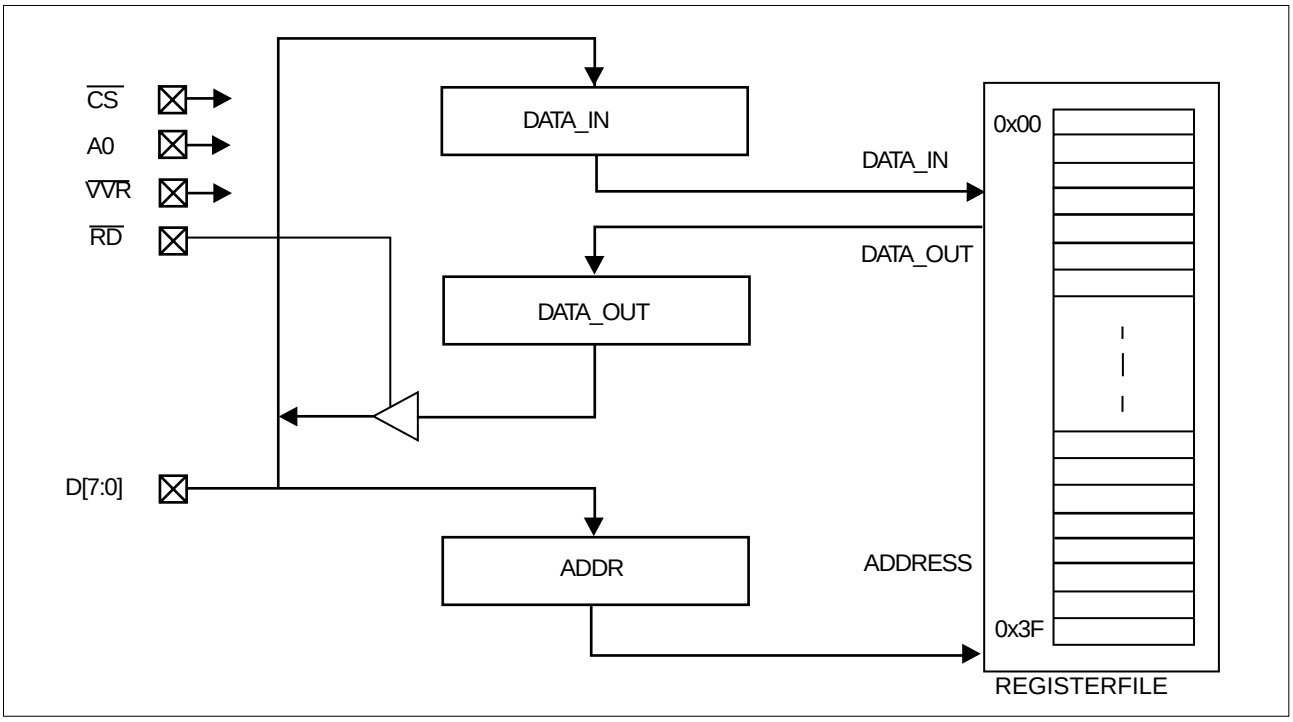
1. The host request a reverse channel transfer by setting nINIT low
2. The peripheral signals that it is OK to proceed by setting PE low
3. The peripheral places data on the data lines and indicates a data cycle by setting BUSY high
4. Peripheral asserts nACK low to indicate valid data
5. Host acknow ledges by setting nAUTOFD high
6. Peipheral sets nACK high. This is the edge that should be used to clock the data into the host
7. Host sets nAUTOFD low to indicate that it is ready for the next byte
8. The cycle repeats, but this time it is a command cycle because BUSY is low

3-4-2 USB INTERFACE

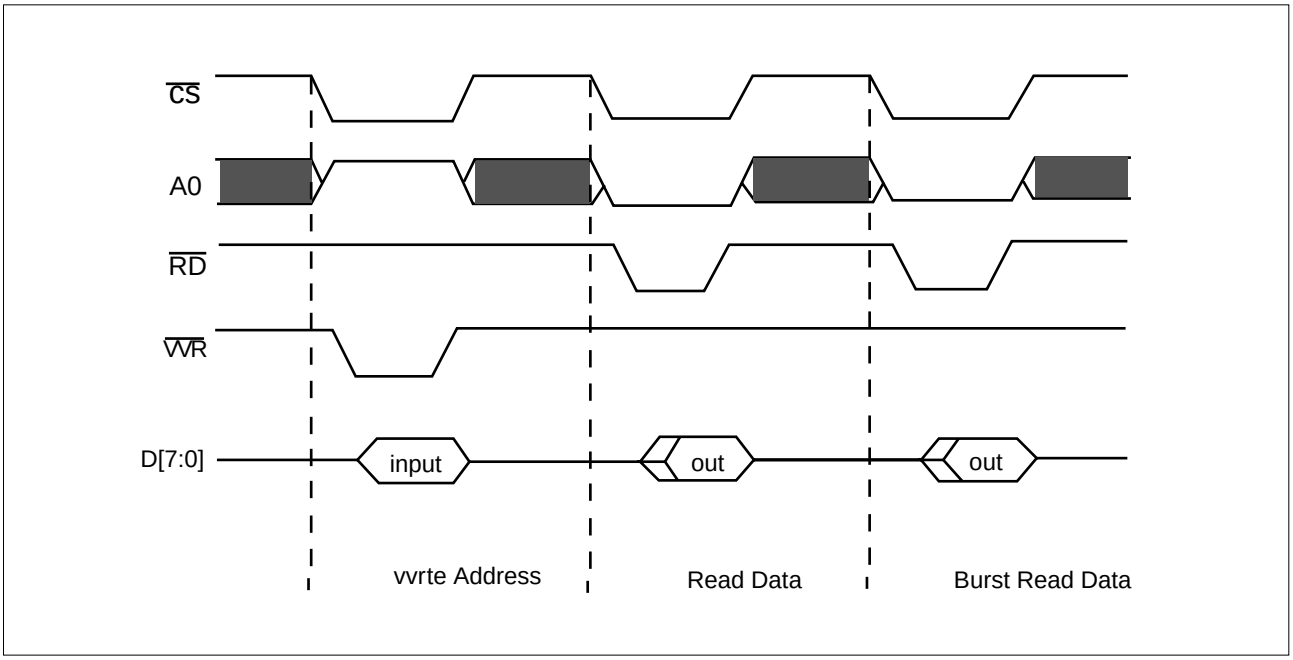


3-4-2-1 Features

- Full-Speed USB Node Device
- USB transceiver
- 3.3V signal voltage regulator
- 48 MHz oscillator circuit
- Programmable clock generator
- Serial Interface Engine consisting of Physical Layer In-terface (PHY) and Media
- Access Controller (MAC), USB Specification 1.0 compliant
- Control/Status Register File
- USB Function Controller with seven FIFO-based End-points :
- One bidirectional Control Endpoint 0 (8bytes)
  - Three Transmit Endpoints (2*32 and 1*64 bytes)
- Three Receive Endpoints (2*32 and 1*64 bytes)
- 8-bit parallel interface with two selectable modes :
  - non-multoplexed
- multiplexed (Intel compatible)
- DMA support for parallel interface
- MICROWIRE/PLUS Interface
- 28-pin SO package



<Non-Multiplexed Mode Interface Block Diagram>



<Non-Multiplexed Mode Basic Timing Diagram>

3-5 Engine Controller

3-5-1. Fuser Control / Thermistor Circuit

This circuit controls the heat lamp temperature to fix the transferred toner on the paper. It is comprised of the thermistor that has the negative resistance against the temperature and LM393 (voltage comparator) and transistor for switching.
The thermistor has the resistance value reverse proportional to the heat lamp surface temperature. The voltage value is read by #60 pin(AVIN2) of CPU refering to the parallel combined resistance with the resistor(R43) connected parallel to it and the voltage distribution of R29. The voltage read activates (inactivates) 'fuser' signal to high (or low) referring to the set temperature and when the 'fuseron' signal turns down(high) to low(high) by Q3 switching, the S21ME4 inside SMPS (PC3) turns on(off) and this eventually turns two-way thyristor(SY1) on(off) to allow(shut) AC voltage to the heat lamp.

LM393 is a H/W designed to protect the system when the software heat lamp control does not run normal. When the thermistor temperature goes up to 210°C, #1 pin's level (LM393) will turn low to turn the 'fuseron' signal to high. (forcefully shuts off Q3)In other words LM393 shuts off the heat lamp forcefully.

3-5-2. Paper Sensing Circuit

1) Cover Open Sensing

Cover Open Sensor is located on the right rear side of the printer. In case the right cover is open, it shuts +5V (LSU laser unit) and +24V(main motor, polygon motor of fixer LSU and HVPS) that are supplied to each unit. It detects the cover opening through CPU. In this case, the red LED of the OP Panel LED will turn on.

2) Paper Empty Sensing

The paper empty sensor (photo interruptor), located inside bottom of the bin cassette detects paper with the actuator connected to it and informs the CPU of whether there is paper. When there is no paper in the cassette, the red LED of the OP panel LED will turn on to tell the user to fill the cassette with papers.

3) Paper Feeding When the paper is fed into the set and passes through the actuator of the feed sensor unit, transistor inside the photo interrupter will turn on, 'nFEED' signal will turn low and inform CPU that the paper is currently fed into the system. CPU detects this signal and sprays video data after certain time (related to paper adjustment). If the paper does not hit the feed sensor within certain time, CPU detects this and informs as "Paper Jam0" (red LED on the OP panel will turn on).

4) Paper Exit Sensing

The system detects the paper going out of the set with the exit sensor assembled to the actuator attached to the frame. If CPU does not turn back high a while after the paper hits the exit sensor, CPU detects this and inform as "Paper Jam2" (red LEDs on the OP panel will turn on).

3-5-3. LSU Circuit

1) Polygon Motor Unit (actuated by +24V)

The polygon motor inside LSU rotates by the 'PMOTOR' signal. When it reaches the motor constant velocity section through the initial transient (transient response) section, it sends the 'nLREADY' signal to the CPU.

The 'clock' pin is the pin that receives clock of the required frequency when LSU uses external CLK as the motor rotational frequency. Currently the external clock circuit is located in the HVPS and 1686Hz = 6.9083MHz (crystal frequency)÷212(74HC4060N IC), is used as the rotational frequency of the polygon motor.

2) Laser Unit (actuated by +5V)

After laser is turned on by 'nLD_ON' signal, it is reflected by 6 mirrors (polygon mirror) attached to the polygon motor and performs scan in horizontal way.When the laser beam hits the corner of the polygon mirror, it generates 'nHSYNC' signal (pulse) and the CPU forms the left margin of the image using this signal (horizontal synchronous signal).

3-5-4. Fan/Solenoid Actuation Circuit

The fan actuation circuit its power using NPN TR. When it receives 'FAN' signal from the CPU. The TR will turn on to make the voltage supplied to the fan to 24V in order to actuate the fan.
The solenoid is actuated in the same way. When it receives control signal from the CPU, the solenoid for paper feeding is actuated by switching circuit.
D29(1N4003) diode is applied to the both ends of the output terminal to protect Q22(KSC1008-Y) from noise pulse induced while the solenoid is de-energized.

3-5-5. PTL Actuation Circuit

PTL actuation circuit switches its power using NPN TR.

3-5-6. Motor Actuation Circuit

Motor actuation circuit is determined while selecting the initial driver IC (provided by the vendor). This system uses TEA3718(U57, U58), A2918(U59)'s motor driver IC. However, the sensing resistance (R273, R274, R292, R293) and reference resistance (R284, R289, R294, R295) can vary depending on the motor actuation current value.
It receives motor enable signal (2 phase) from CPU and generates bipolar pulse (constant-current) and sends its output to stepping motor input.

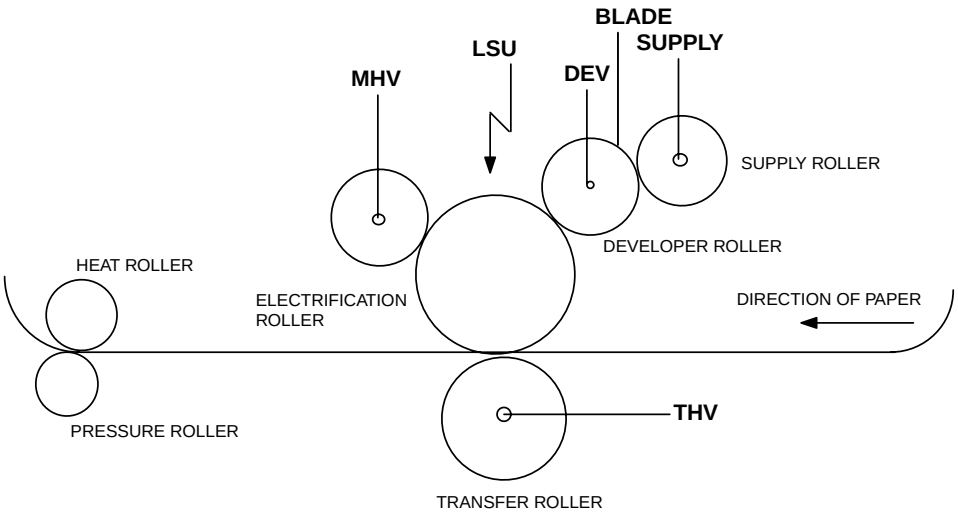
3-5-7. High Voltage Power Supply

3-5-7-1. Summary

It is the high voltage power supply that has DC+24V/DC+5V (used for the image forming device in OA digital picture developing method) as the rated inputs. It supplies electrifying voltage (MHV), supply voltage (SUPPLY), developing voltage (DEV), blade voltage(BLADE) and transferring voltage (THV).
Each high voltage supply shows the voltage required in each digital picture process.

3-5-7-2. Digital Picture Process

Digital picture developing method is widely used by copy machine, laser beam printer and fax paper.
The process is comprised of electrification, exposure, develop, transfer and fixing.

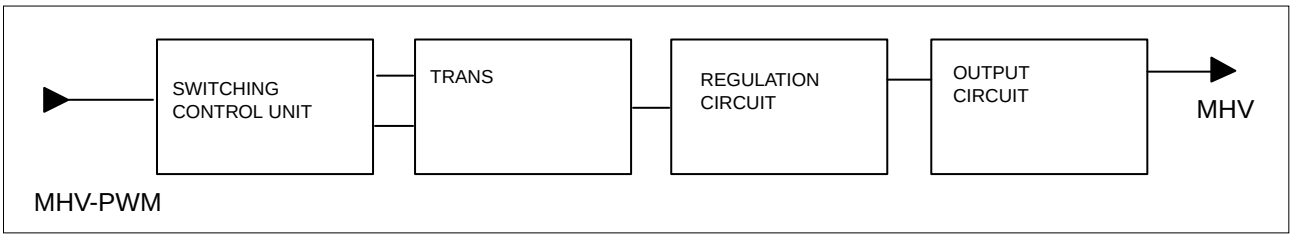


First, in the electrification process, retain constant charge at approx. -900V for the electric potential on the OPC surface by electrifying OPC drum at approx. -1.4KV through the electrification roller.
The electrified surface of OPC is exposed responding to the video data by the LSU that received print command due to rotation. The unexposed non-video section will retain the original electric potential of -900V, but the electric potential of the image area exposed by LSU will be approx. -180V that it will form the electrostatic latent image. The surface of the photo-conductive drum where the electrostatic latent image is formed reaches the developer as the drum rotates. Then the electrostatic latent image formed on the OPC drum is developed by the toner supplied to the developing roller by supplying roller and it is transformed into visible image. It is the process to change the afterimage on the OPC drum surface formed by LSU into visible image by the toner particles.
While the supply roller energized with -450V by HVPS and the developer roller energized with -300V rotate in the same direction, it keeps the toner particles between two rollers supplied to OPC drum in negative state by the friction between two rollers.
The toner supplied to the developer roller is biased to bias electric potential by the developer roller and transferred to the developing area. After (-) toner is attached to the developer roller, it will move to the exposed high electric potential surface (-180V) rather than to the unexposed low electric potential surface (-900V) of the developer roller and OPC drum. Eventually the toner will not settle in the low electric potential surface to form the visible image.
Later, the OPC drum continues to rotate and reaches to transfer location in order to accomplish the transfer process.
This process transfers the (-)toner on the transfer roller to the printing paper by the transfer roller. The (-)toner attached to the OPC drum will be energized to hundreds to thousands of the (+)transfer voltage by HVPS. The (+)electrostatic force of the transfer roller generated has higher adhesiveness than the (-)toner OPC drum and thus it moves to the surface of the paper passing through the transfer roller.
The toner transferred to the paper with weak electrostatic force is fixed to the paper by the pressure and heat of the fixer composed of pressure roller and heat roller.
The toner attached to the paper is melted by applying the heat (approx. 180°C) from the heat roller and the pressure (approx. 4kg) from the pressure roller. After the fixing process, the paper is sent out of the set to finish the printing process.

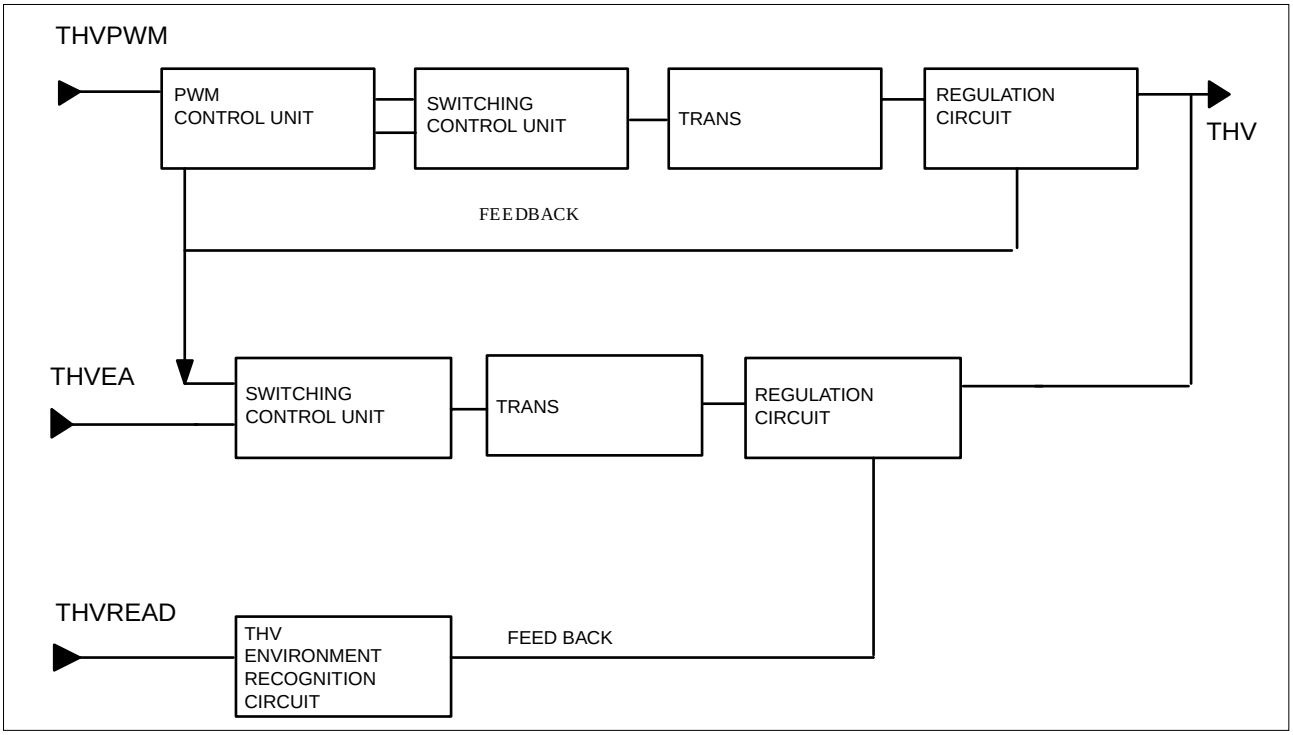
3-5-7-3. Organization of the Device

HVPS is comprised of electrification output unit, bias output unit and transfer output unit.

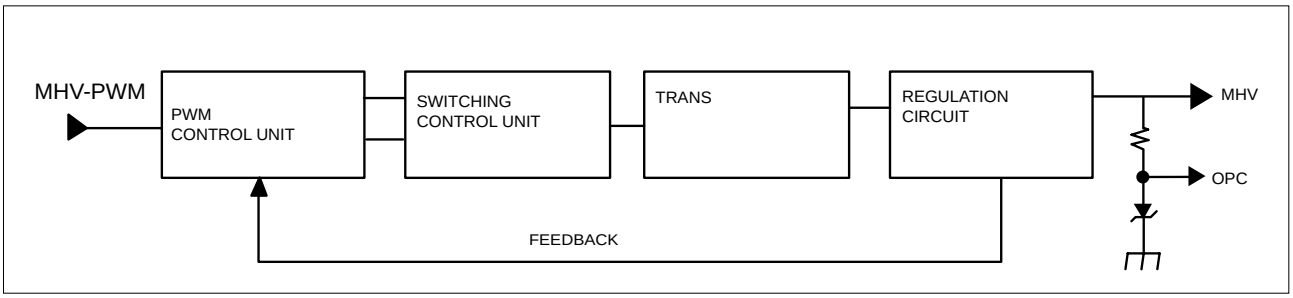
1) Input Unit
2) Electrification Output (Enable) Unit: MHV (Main High Voltage)
3) Bias Output (Enable) Unit: DEV (Development Voltage)/Supply(Supply Voltage)/BLADE(Blade Voltage)
4) Transfer '+' Output (Enable) Unit: THV(+)(Transfer High Voltage(+))
5) Transfer '-' Output (Enable) Unit: THV(-)(Transfer High Voltage(-))
6) Switching Unit
7) Feedback Unit
8) Regulation Unit
9) Output Unit



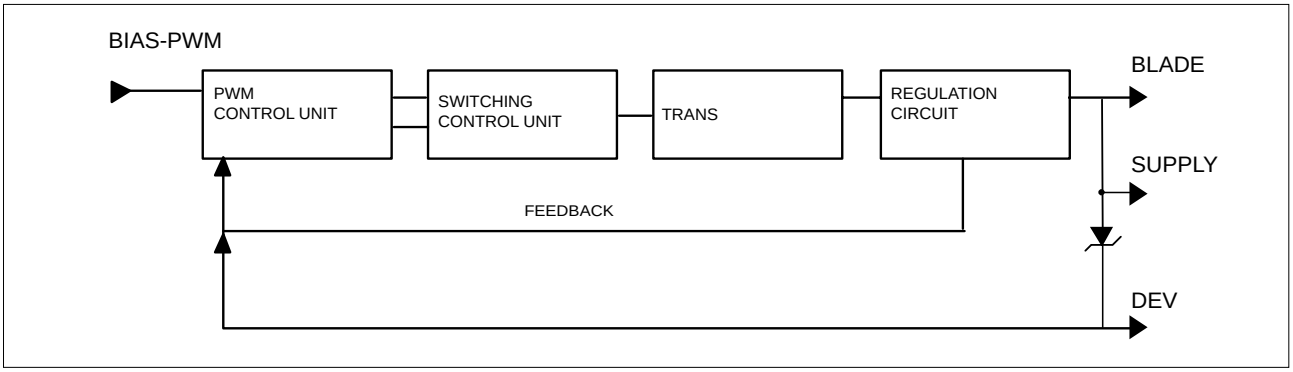
<Electrification Unit Block-Diagram>



<Transfer Output Unit Block Diagram>



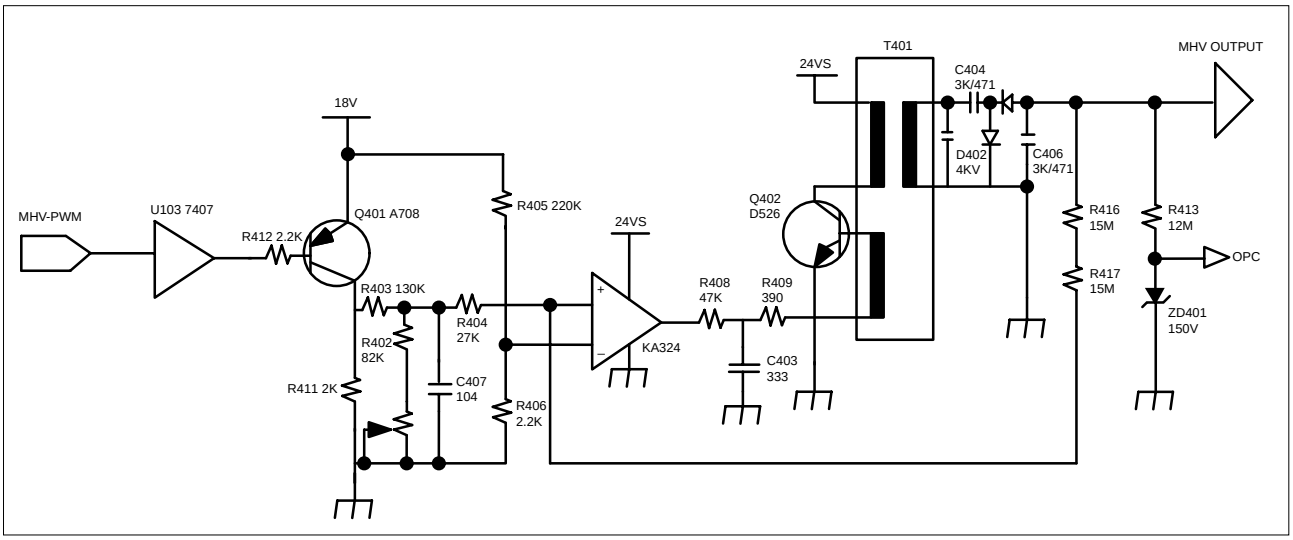
<MHV Output unit Block Diagram>



<BIAS Output Unit Block Diagram>

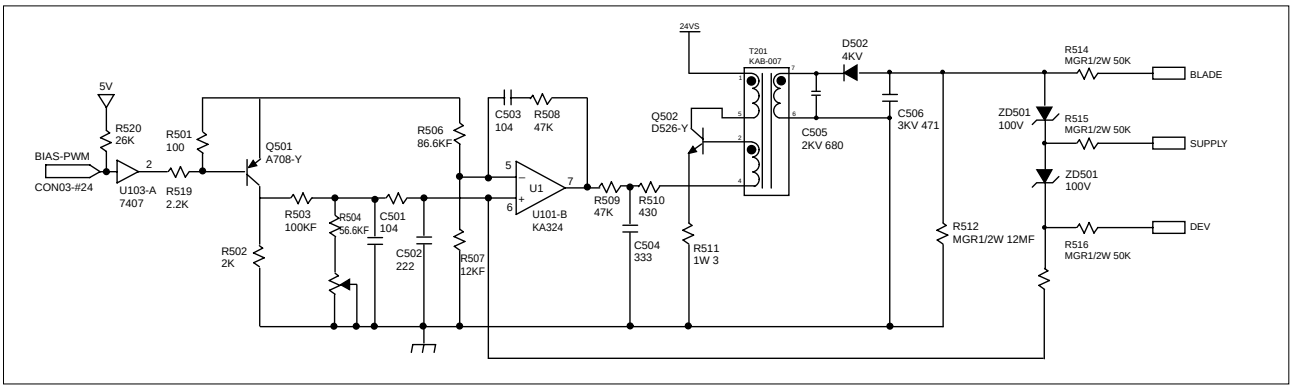
3-5-7-4 MHV (Electrification Output Enable)

Electrification Output Enable is the electrification output control signal 'PWM-LOW ACTIVE'.
When MHV-PWM LOW signal is received, Q401 turns on and the steady voltage will be accepted to the non-inverting terminal of OP-AMP 324. As the voltage higher than the inverting reference voltage of OP-AMP, which is set to R405 and R406, OP-AMP output turns high. This output sends IB to the TRANS auxiliary wire through current-restricting resistance Q402 via R408 and C403 and Q402 turns on. When the current is accepted to Q402, Ic increases to the current proportional to time through the T401 primary coil, and when it reaches the Hfe limit of Q402, it will not retain the "on" state, but will turn to "off". As Q402 turns 'off', TRANS N1 will have counter-electromotive force, discharge energy to the secondary unit, sends current to the load and outputs MHV voltage through the high voltage output enable, which is comprised of Regulation– circuit.



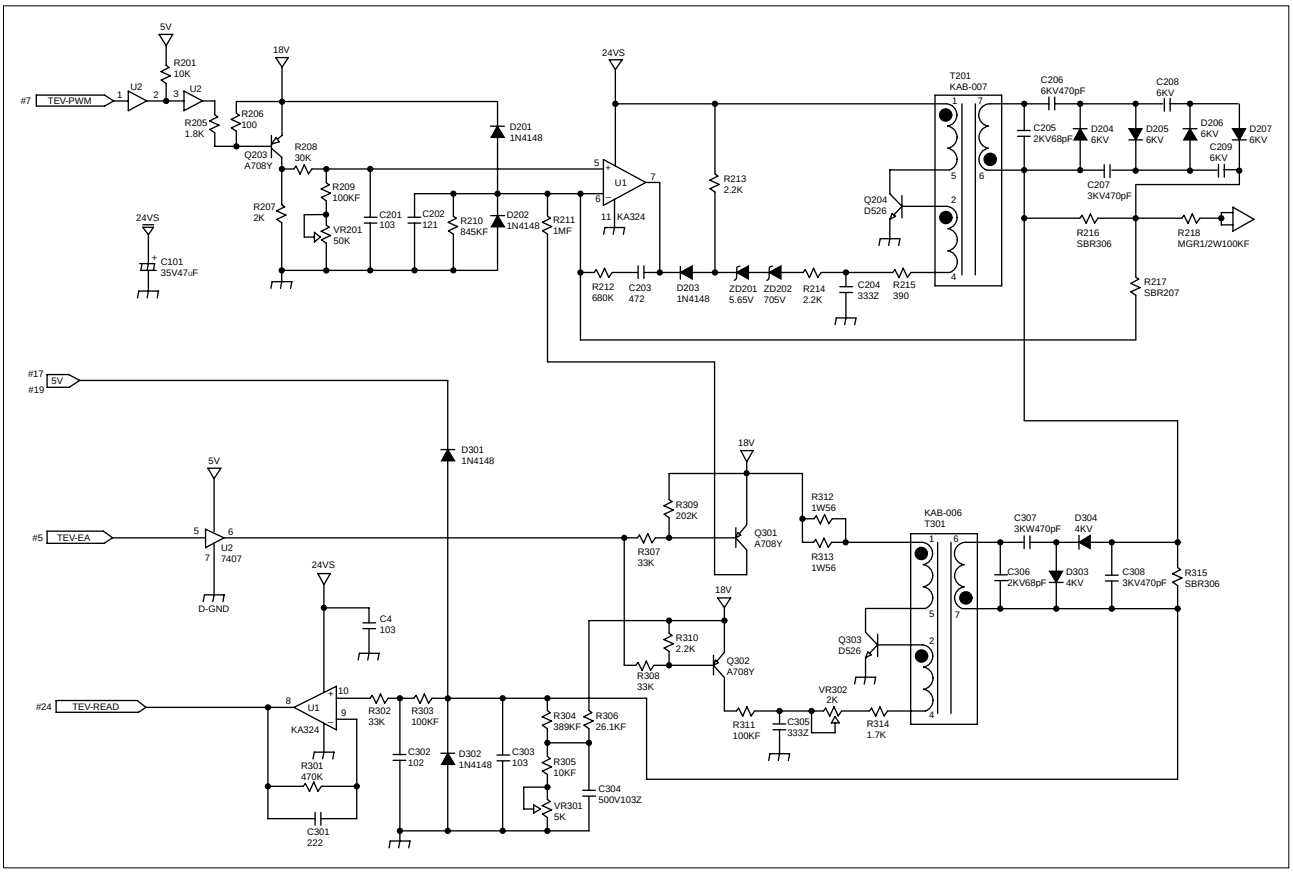
3-5-7-5 BIAS (supply/dev/blade output unit)

BIAS (Electrification Output Enable)Electrification Output Enable is the electrification output control signal 'PWM-LOW ACTIVE'.When BIAS-PWM LOW signal is received, Q501 turns on and the steady voltage will be accepted to the non-inverting terminal of OP-AMP 324. As the voltage higher than the inverting reference voltage of OP-AMP, which is set to R506 and R507, OP-AMP output turns high. This output sends IB to the TRANS auxiliary wire through current-restricting resistance Q502 via R509 and C504 and Q502 turns on. When the current is accepted to Q502, Ic increases to the current proportional to time through the T201 primary coil, and when it reaches the Hfe limit of Q502, it will not retain the "on" state, but will turn to "off". As Q502 turns 'off', TRANS N1 will have counter-electromotive force, discharge energy to the secondary unit, sends current to the load and outputs DEV voltage through the high voltage output enable, which is comprised of Regulation-circuit.



3-5-7-6. THV(THV(+)/THV(-) Output Unit)

Transfer(+) output unit is the transfer output control signal 'PWM-LOW ACTIVE'.
When THV-PWM LOW signal is received, Q203 turns on and the steady voltage will be accepted to the non-inverting terminal of OP-AMP 324. As the voltage is higher than the inverting reference voltage of OP-AMP, OP-AMP output turns high.
The 24V power adjusts the electric potential to ZD201 and ZD202, sends IB to TRANS auxiliary wire through current-restricting resistance R215 via R212 and C204, and eventually Q204 will turn on. When the current is accepted to Q402, Ic increases to the current proportional to time through the T201 primary coil, and when it reaches the Hfe limit of Q204, it will not retain the "on" state, but will turn to "off". As Q402 turns 'off', TRANS N1 will have counter-electromotive force, discharge energy to the secondary coil, sends current to the load and outputs THV voltage through the high voltage output enable, which is comprised of Regulation– circuit. The output voltage is determined by the DUTY width. Q203 switches with PWM DUTY cycle to fluctuate the output by fluctuating the OP-AMP non-inverting end VREF electric potential, and the maximum is output at 0% and the minimum, at 100%.Transfer(-) output unit is THV-EA 'L' enable.
When THV-EA is 'L', Q302 turns on and the VCE electric potential of Q302 will be formed and sends IB to TRANS auxiliary wire through R311, C305 and VR302 via current-restricting resistance R314, and eventually Q303 will turn on. When the current is accepted to Q303, Q303's Ic increases to the current proportional to time through the T301 primary coil, and when it reaches the Hfe limit of Q303, it will not retain the "on" state, but will turn to "off". As Q303 turns 'off', TRANS N1 will have counter-electromotive force, discharge energy to the secondary coil, send current to load and output THV(-) voltage through the high voltage output enable, which is comprised of Regulation– circuit.



3-5-7-7. Environment Recognition

THV voltage recognizes changes in transfer roller environment and allows the voltage suitable for the environment in order to realize optimum image output. The analog input is converted to digital output by the comparator that recognizes the environmental changes of the transfer roller. It is to allow the right transfer voltage to perform appropriate environmental response considering the environment and the type of paper depending on this digital output by the programs that can be input to the engine controller ROM.

This environment recognition setting is organized as follows: First, set the THV(+) standard voltage.
Allow 200MΩ load to transfer output, enable output and set the standard voltage 800V using VR201.
Then set 56 (CPU's recognition index value) as the standard using VR302.
This standard value with CPU makes sure that the current feedback is 4μA when output voltage is 800V and load is 200MΩ.
If the load shows different resistance value when 800V is output, the current feedback will also be different and thus the index value will also be different. according to the index value read by CPU, the transfer voltage output will differ according to the preset transfer table.
The changes in transfer output required by each load is controlled by PWM-DUTY.

3-6 OPE PBA

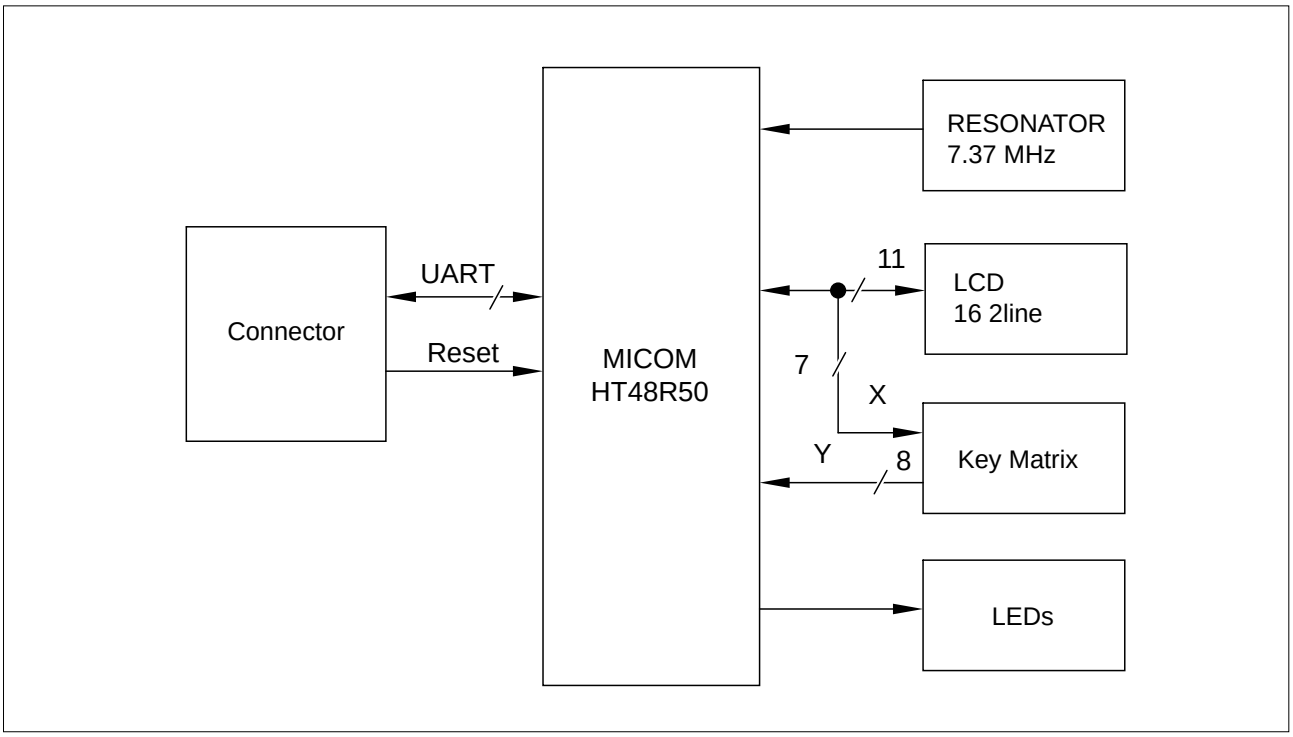
3-6-1 SUMMARY

OPE Board is separated functionally from the main board and operated by the micom(HT48R50) in the board. OPE and the main use UART (universal asynchronous receiver/transmitter) channel to exchange information. OPE reset can be controlled by the main. OPE micom controls key-scanning and LCD and LED display. If there occurs an event in OPE (such as key touch), it sends specific codes to the main to respond to the situation and the main analyzes these codes and operates the system. For example, it the main is to display messages in OPE, the main transmits data through UART line to OPE according to the designated format and OPE displays this on LCD, LED. OPE's sensing is also transmitted to the main through UART line and then the main drives necessary operation.

OPE PBA consists of U1(MICOM, HT48R50),LCD, key matrix, LED indicators. Refer to OPE Schematic Diagram and Wiring Diagram sections of this manual.

• Signals from the key matrix are delivered to U1 input pin group (D1~D6)
• U1 pin 48 (TX DATA) is the UART code sent to MAIN PBA.

• Display from the controller is received at U1 pin 5(RX DATA).
• LCD drive signals are sent from U1 P2-x pin group, P3-4~P3-6 pins.
• Machine status LED drive signals are sent from U1 LED0~LED7.



<OPE BLOCK DIAGRAM>

3-7 LIU PBA

3-7-1. SUMMARY

LIU WIRE CONNECTS Main B'D's MODEM AND LINE PARTS, AND IMPEDANCE MATCHING (AC, DC), RING DETECTION PART and LINE SEIZURE (DIALER).

3-7-2. DC MATCHING PART

Normal movement range of LIU is 12mA ~ 9mA.
Adapting CTR21 standard, the regulation limits to 60mA CURRENT flow through the terminal.
Therefore, select (*:for EU PIT) Option to connect necessary items then the current through LIU will not exceed 60mA.

• CTR21 Standard(Europe) : 12mA~60mA • OTHER Standard (U.S.) : 12mA~90mA

DC has a character to pass through the LINE. And with Q1 (VN2410) GATE section's LINE INPUT corrent and Q1 Source connection to R20, can be decided as follows :

• -VDCR = VL1 + ILINE X R20

(VDCR : Tip-Ring CD Voltage, ILINE : Current flow)VL1:Line Input Voltage, VL1=VBD1+VCE(Q2)+VDS(Q1)

3-7-3. AC MATCHING PART

Basic LIU's AC IMPEDANCE is 600 and uses R47. 48. C36 to possibly control combined IMPEDANCE.

• U.S. Usage : A terminal IMPEDANCE Æ 600W(±30%)
• CTR21 : A Terminal IMPEDANCE Æ 270+750W//150nF

3-7-4. DIALER PART

***MF DIAL**

DTMF Dialing is controlled by MODEM and should be selected by appropriate LEVEL and On-off Time output based on each countries' own National specification.

• Freq. Tolerance : ±1.5%
High Group : 1209, 1336, 1477, 1633Hz
Low Group : 697, 770, 852, 941 Hz

	U.S. Usage	CTR21
High Freq Level	-9.0+2.0/-2.5	-7.0 +1.0/-2.0
Low Freq Level	-9.0+1.0/-2.0	-11.0+2.5/-2.0

***DP DIAL**

Controls from MAIN through / DP-Terminal.
for U.S.Usage, set time to DF signal of 40:60 M/B. DP signal is made of U6 (pcb817). The DC current which flows thru Q2 Base is regulated by On/Off switch and turns to DP dial signal with a COUPLER.

• CTR 21 does not have telephone capability but has the number 3 and 4 Line Connection. No DP condition but possibility to get approval only on DTMF Dial based terminal.

3-7-5. RING DETECTION PART

RING SIGNALS from the LINE section (TIP, RING)are further passed through C5, R3, ZD1, and ZD2 and ends up at U9, (PC 814). U9 then detects above RING SIGNAL and passes the output to MAIN B'D. The wilre diagram's C5 is RINGER CAPACITOR and it normally uses 1UF/250V.
A R3 limits AC current and controls upper and lower REN meter.

3-8 SMPS (Switching Mode Power Supply) Unit.

3-8-1 SMPS Specifications

The SMPS (Switching Mode Power Supply) Unit used here is a PWM (Pulse Width Modulation) type power supply unit that supplies DC+5V to controller and control panel, and DC+5V, DC+24V and DC+12V to the engine. It also supplies AC power to fixer heat lamp.

No.	Output Channel	Ch.1	Ch.2	Ch.3
1	Channel Name	+5.1V	+24.0V	+12.0V
2	Rated Output Voltage	+5.1V	+24.0V	+12.0V
3	Rate Output Current	2A	2.5A	0.8A
4	Maximum Load Current and Load Pattern	2.5A Continued	3.0A Continued	0.8A Continued
5	Load Change Range	0.5~2.0A	0.1~0.3A	0.1~0.8A
6	Rate output voltage (For rated I/O)	+5.1V±5% (+4.84~+5.35V)	+24.0V±10% (+21.60~+26.40V)	+12V±5% (+11.40~+12.60V)
7	1) Total Output Voltage Deviation (Input, Load, Temp., Aging) 2) Dynamic Input Change 3) Dynamic Load Change	Including All +5.1V±5% (+4.84~+5.35V) Including Set Error	Including All +24.0V±10% (+21.60~+26.40V) Including Set Error	Including All +12V±5% (+11.40~+12.60V) Including Set Error
8	Refer to ripple & noise 27	150mVp-p or less	500mVp-p or less	200mVp-p or less
9	Refer to load short and overload protection 23 Refer to load short and overload protection 23	Must not ignite or generate smoke when output shorted for 5 sec.	Output voltage must shutdown withing the range of 3.5A~6.5A	Must not ignite or generate smoke when output shorted for 5 sec.

3-8-2 AC Input Stage

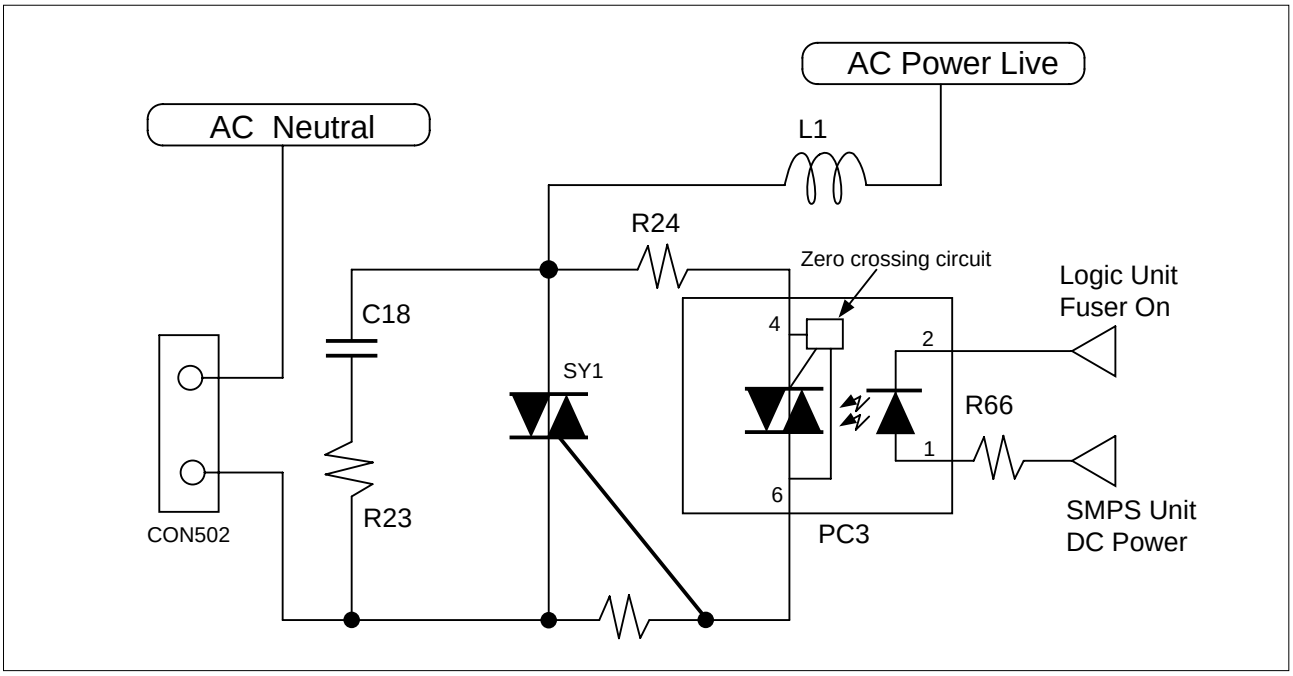
AC Input power path is consist of the Fuse (F1) for AC current limit, the Varistor (TNR1) for by-passing high Voltage Surge, the discharge resistor(R1), the AC Impalse Noise Filtering Circuit (C2, C4, LF1), the Common Mode Grounding Circuit (C5, C6), the 2'nd noise filter (C7, LF2), and the thermistor (TH1).
Wher power is turned on, TH 1 limits Inlush-Current by it's high resistanle, and When it's temperature rise, it's resistance become about Zero ohm.

3-8-3 SMC(Switched Mode Control)

The AC input voltage is rectified and filtered by BD1 and C10 to create the DC high voltage applied to the primary winding of T1, Q5 pin #1 is driven by the SMPS device IC2, IC2. auto-starts and chops the DC voltage. The U502 is PWM SMPS IC and has internally a SMC(switched mode control) IC and a MOSFET output stage. The SMC IC has a Auto-restart without a Power Supply for the IC and a Thermal Shutdown function and so on. R4, R5, C11, D1 clamp leading-edge voltage spikes caused by transformer leakage inductance. The power secondary winding(Pin #5~6)is rectified and filtered by D8, D9, L2, C33, C34 to create the 5V output voltage. The bias winding(Pin #9~8)is rectified and filltered by D2 and C12 to create U502 bias voltage. The secondary output 5V is regulated through the path of the voltage divide by R34, R35.

3-8-4. Fixed Temperature Control

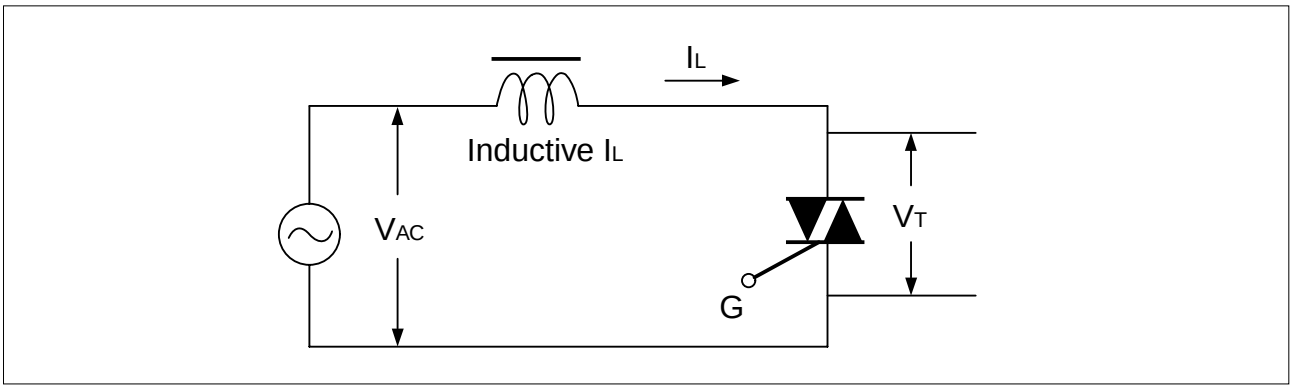
3-8-4-1. Fixed Lamp Control Circuit



<Fixed Lamp Control Circuit>

3-8-4-2. The Concept of Fixed Lamp Control

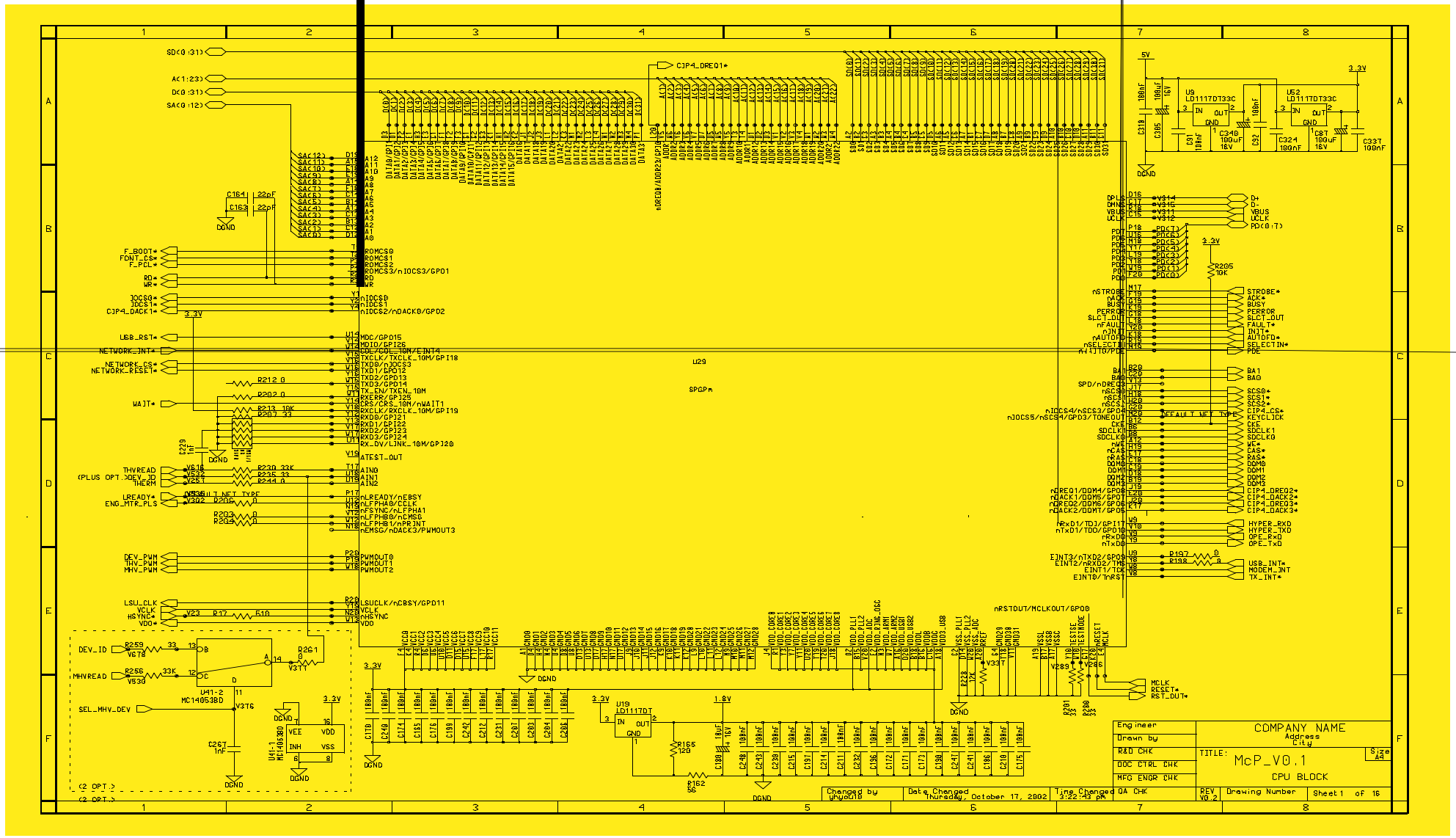
For fixed lamp control, the logic unit "fuser on" control signal and SMPS unit DC power must be supplied. This circuit turns on only when "fuser on" sends the signal and the DC power is supplied.
The following explains how the fixed lamp control circuit works.
logic unit "fuser on" sends trigger current to triac driver PC3 LED, then the infrared ray is detected by PC3 photo detector. Next, YC3 triac is conducted.
The conducted current sends trigger input to triac SY1 gate. At this point, SY1 is conducted and AC power is supplied to fixed lamp. Lamp is turned on and temperature rises.
As this fixed lamp control circuit uses the AC voltage ("+" and "-" are repeated) as the power supply, it used two-way triac (SY1), which has advantage over one-way SCR considering the price, size and reliability.
Triac's gate can be triggered by either forward or reverse signal. Once triac is turned on, it will not be controlled by gate signal, but will be continuously on until the current between major terminals decreases below the holding current. In other words, you cannot turn it off with reverse signal unlike SCR. This property is called current-voltage threshold rise rate (commutation: dv/dt). In AC power control application, triac has to turn off conduction in each zero crossing or switch it twice in each cycle. This switching operation is called commutation. It is possible to turn off the triac at the end of half cycle by eliminating the gate signal when the load current (IL) is gained at the level equal to or lower than holding current. When triac commutes off-line, the direction of the voltage of the both ends of triac will be reversed and increase up to the maximum value of line voltage (VAC). At this point, the width of rise rate will be determined by dv/dt and overshoot voltage, by the circuit. When triac commutes off-line, the voltage of both ends of triac will have the same voltage as the line voltage.



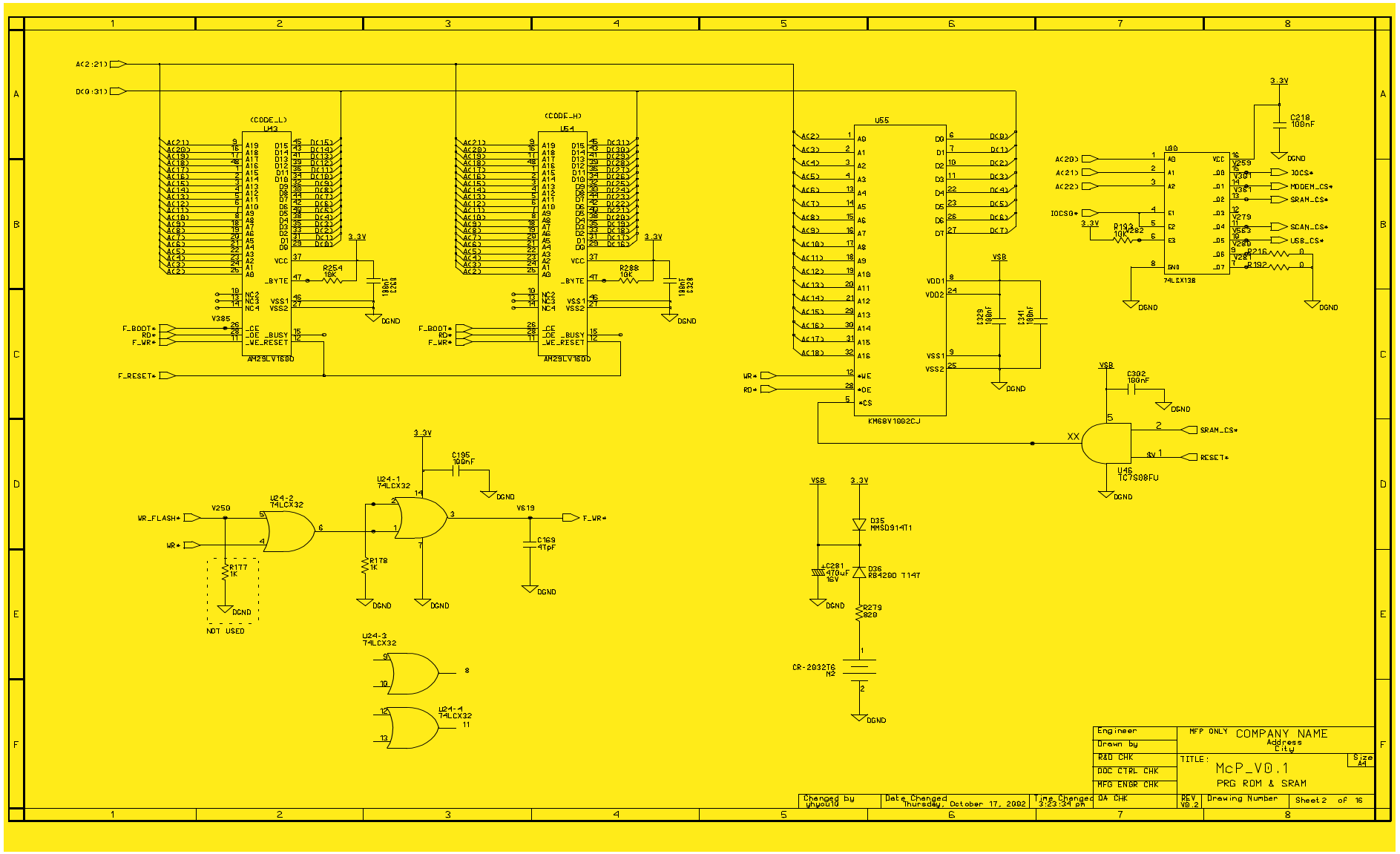
<Inductive Circuit>

4. Schematic Diagrams

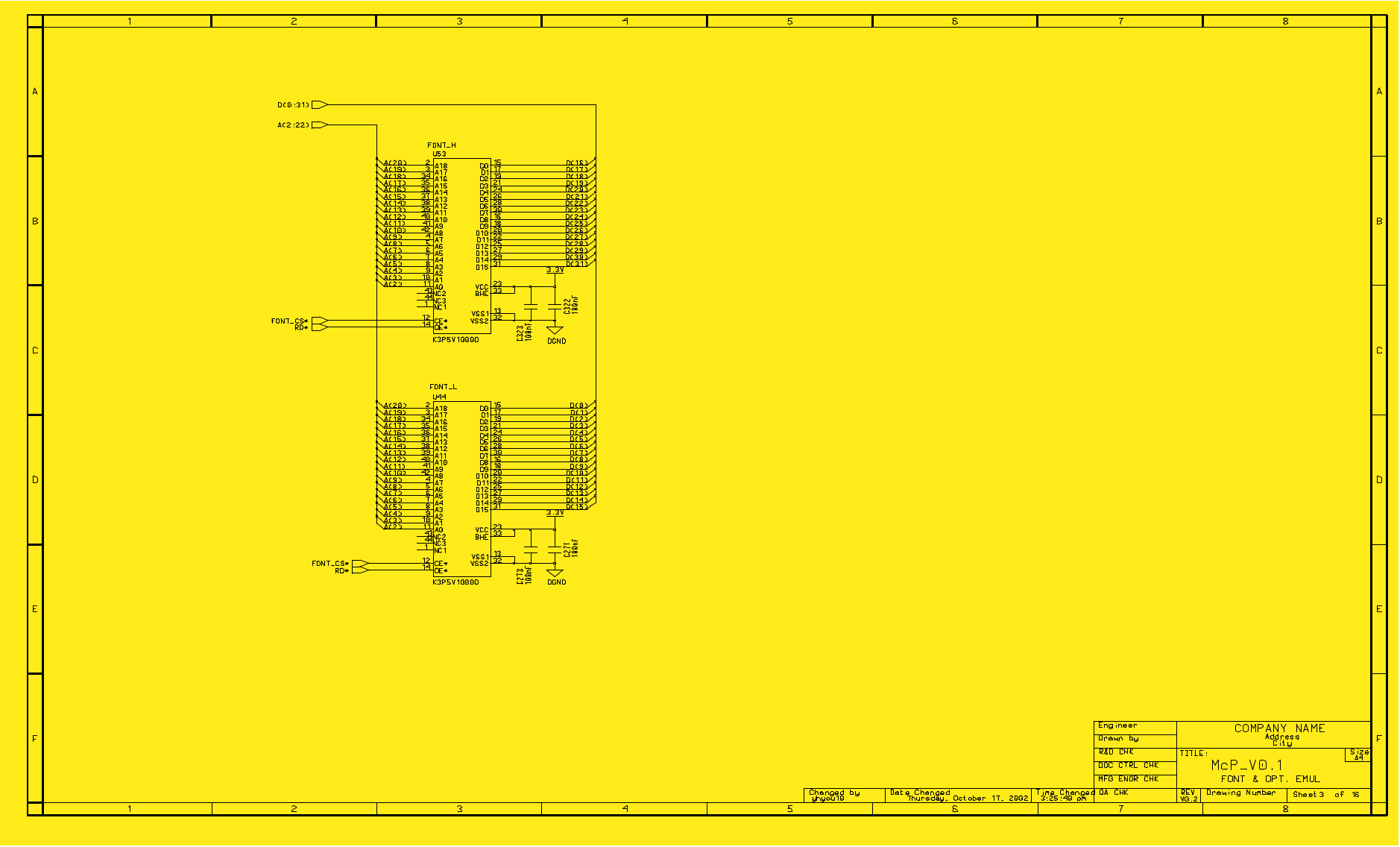
4-1 Main Circuit Diagram (1/16)



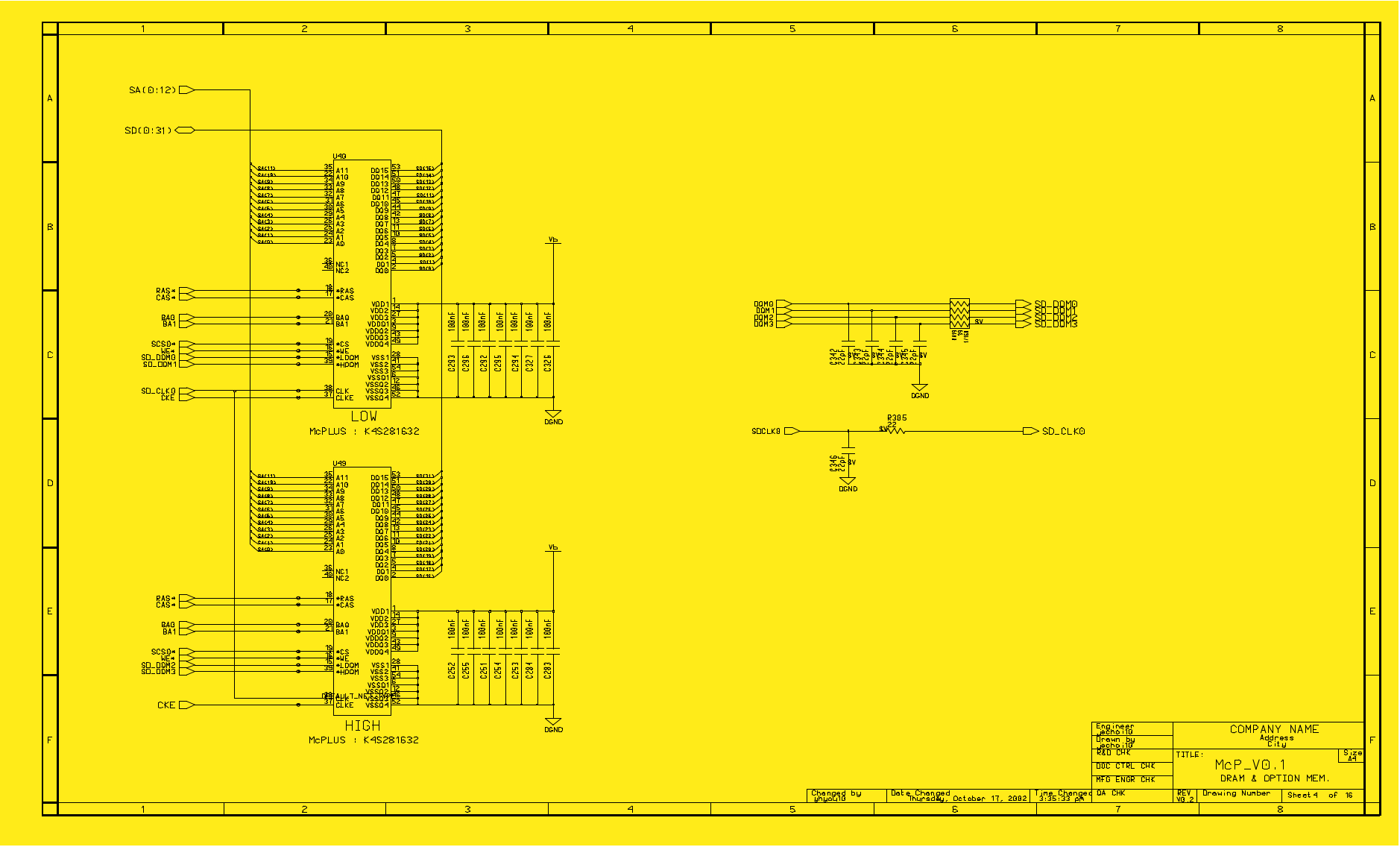
Main Circuit Diagram (2/16)



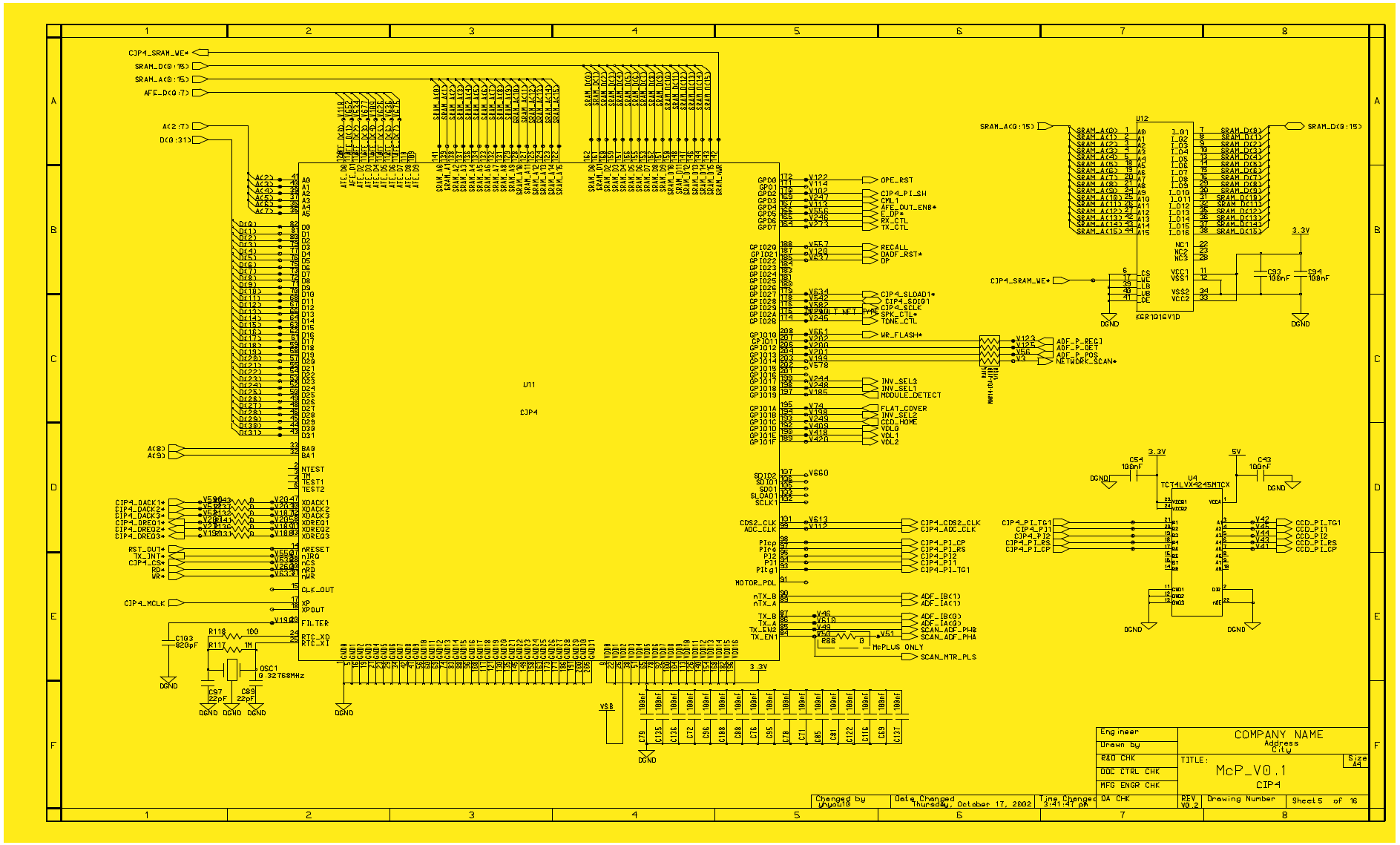
Main Circuit Diagram (3/16)



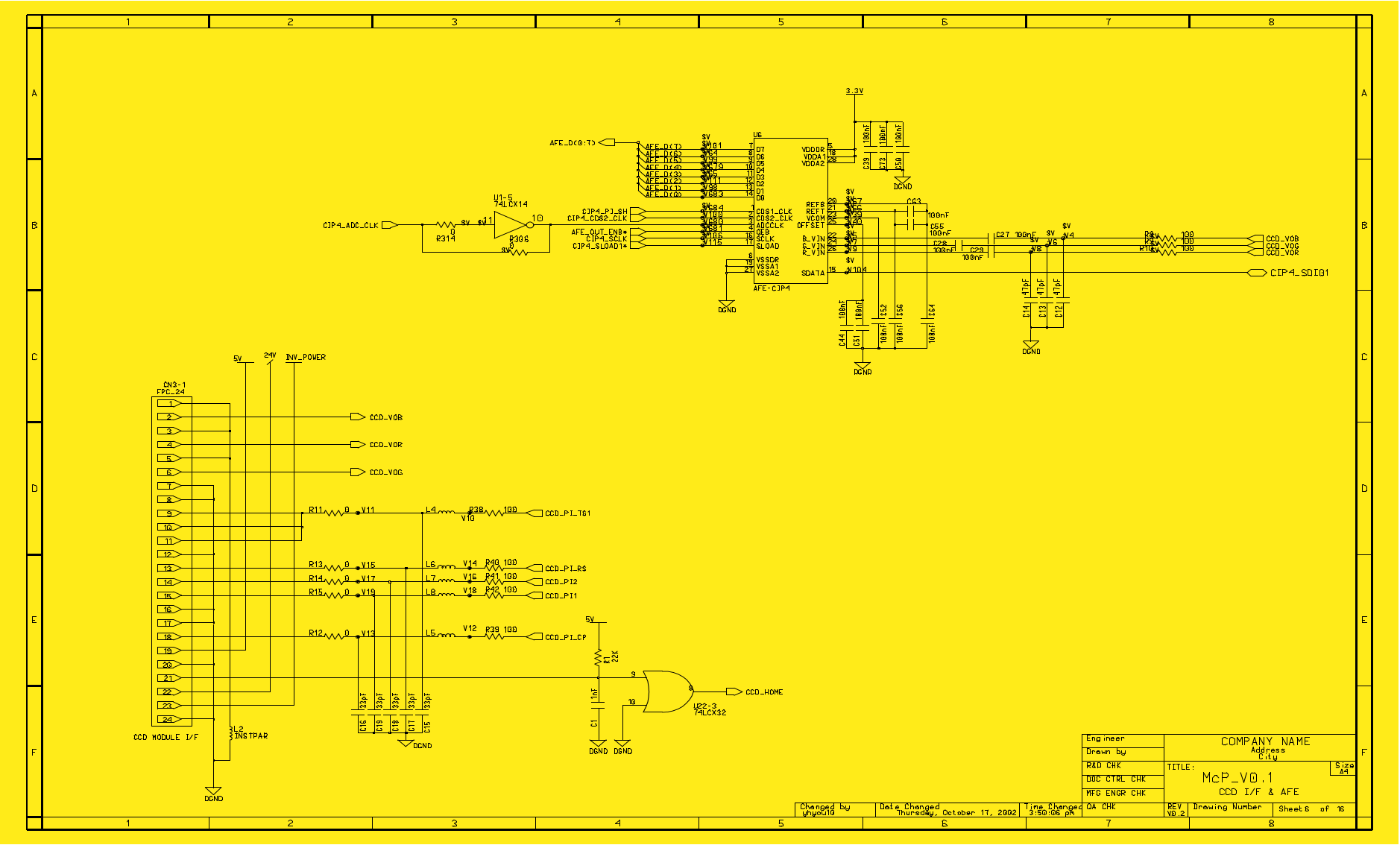
Main Circuit Diagram (4/16)



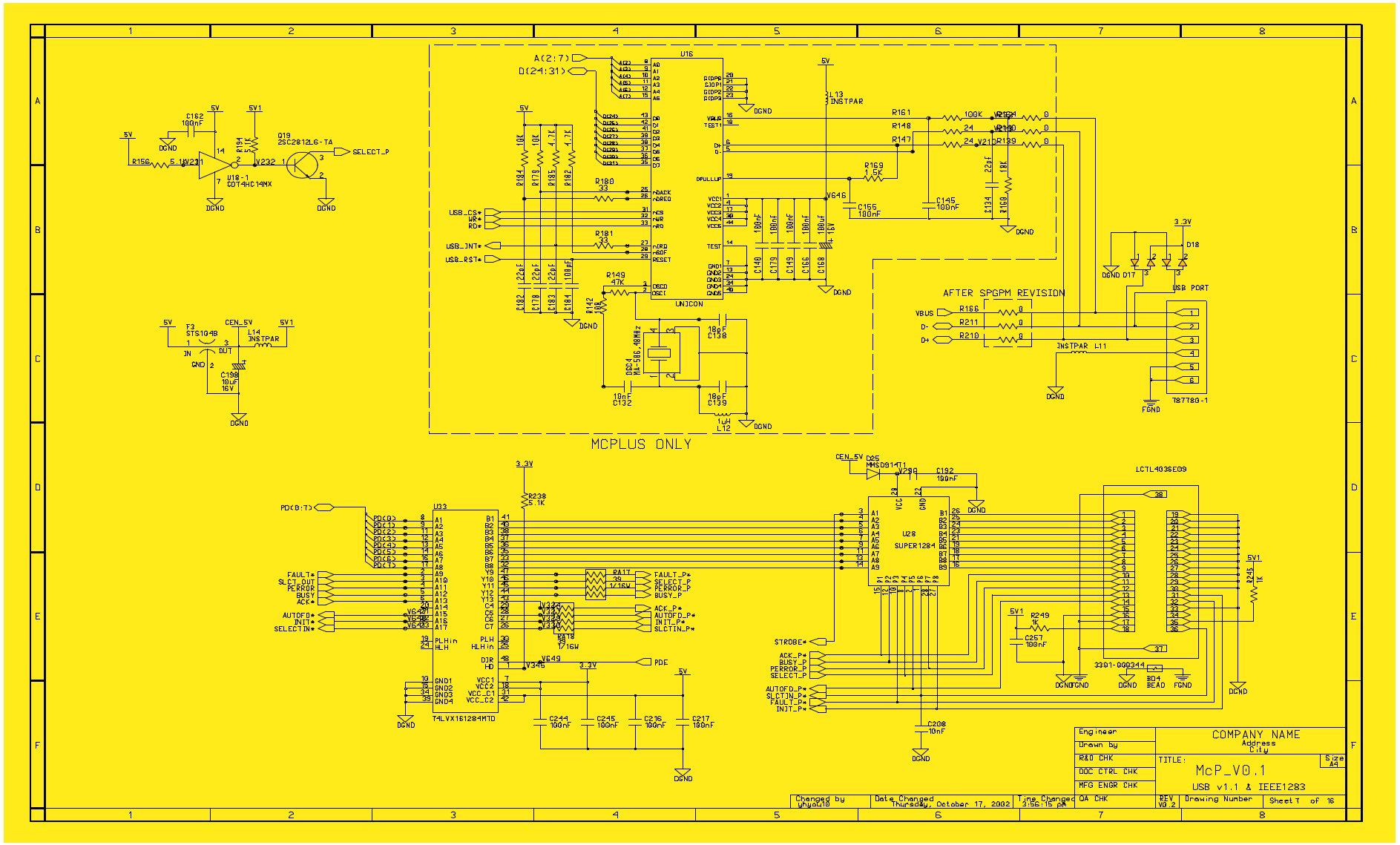
Main Circuit Diagram (5/16)



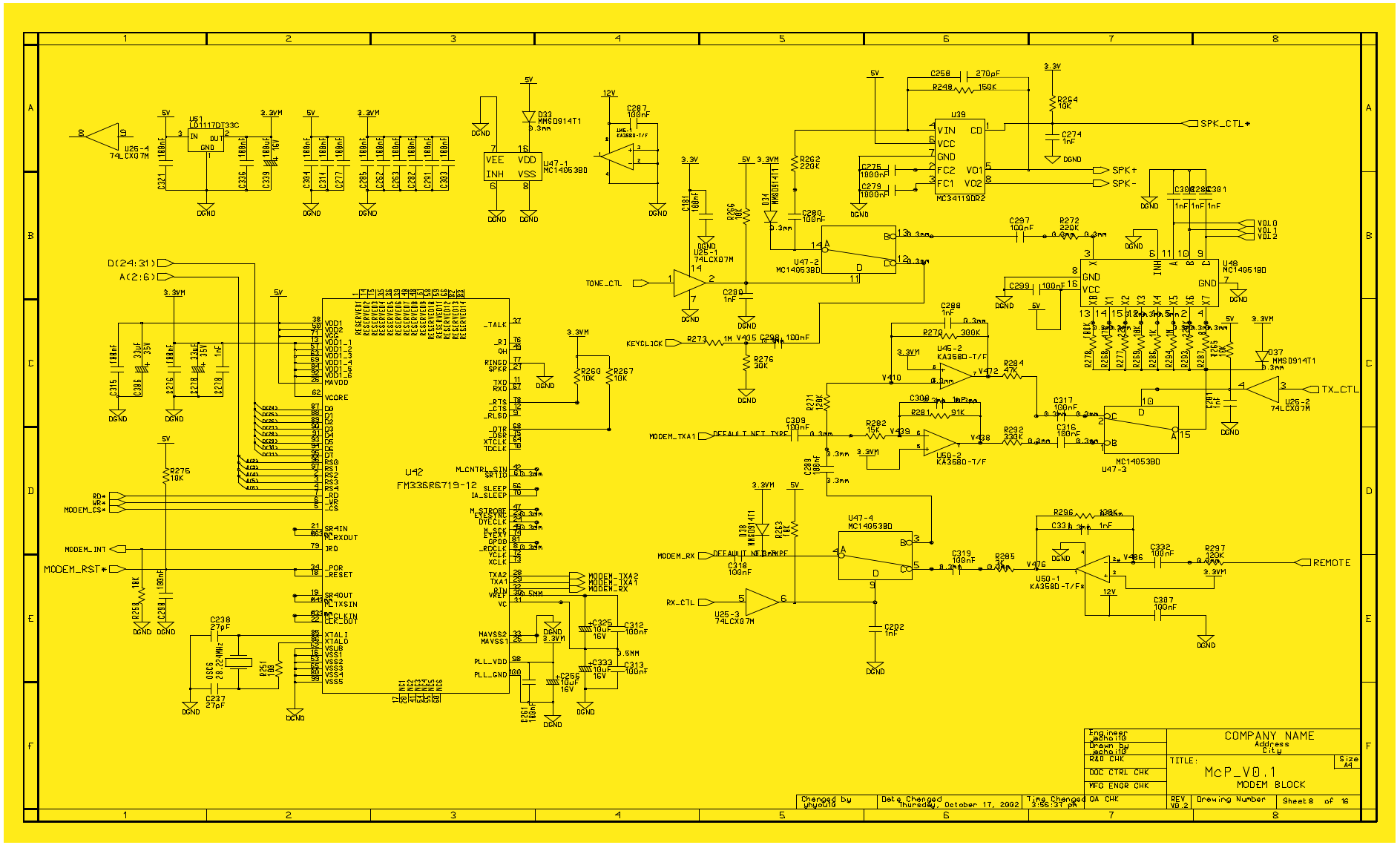
Main Circuit Diagram (6/16)



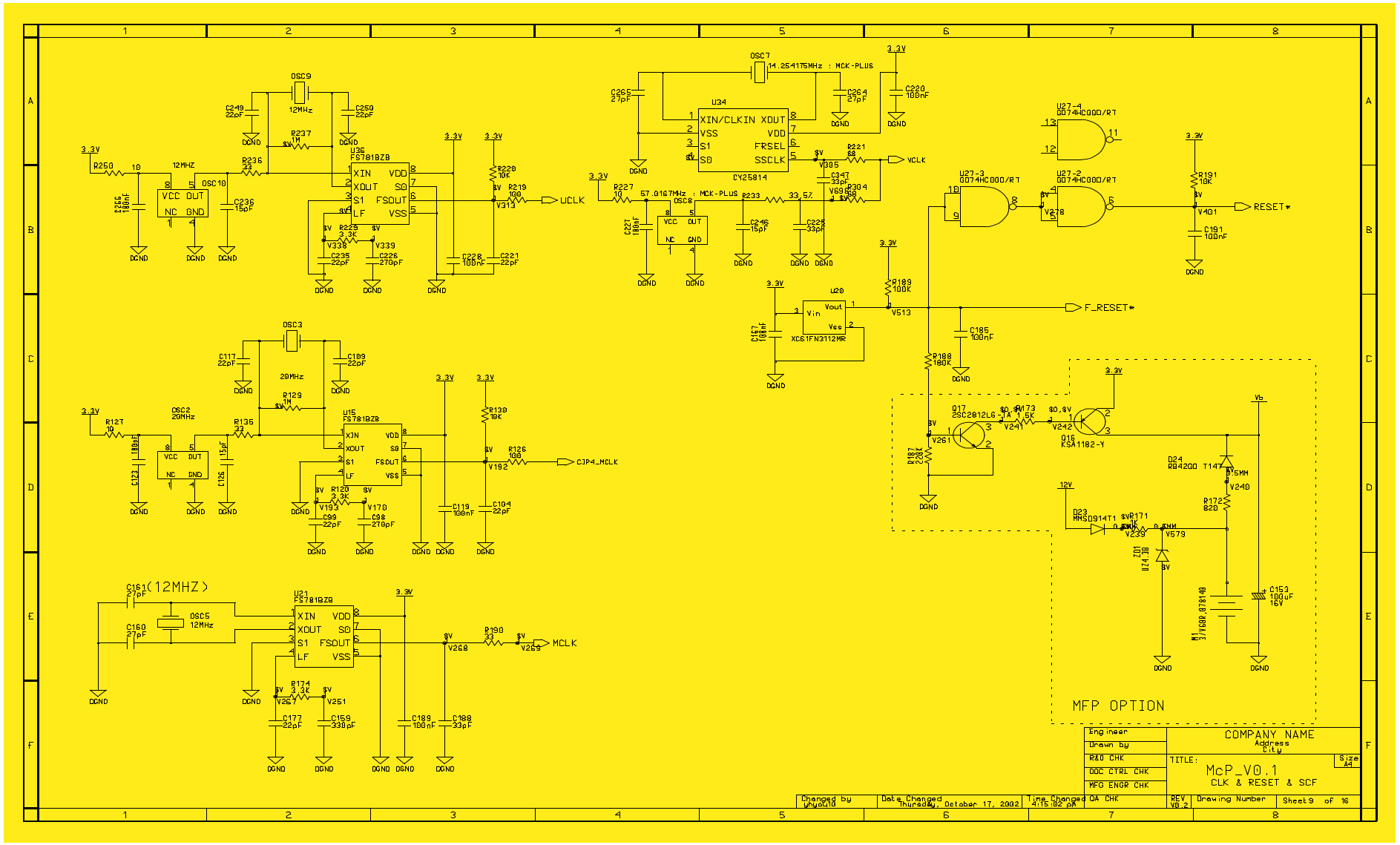
Main Circuit Diagram (7/16)



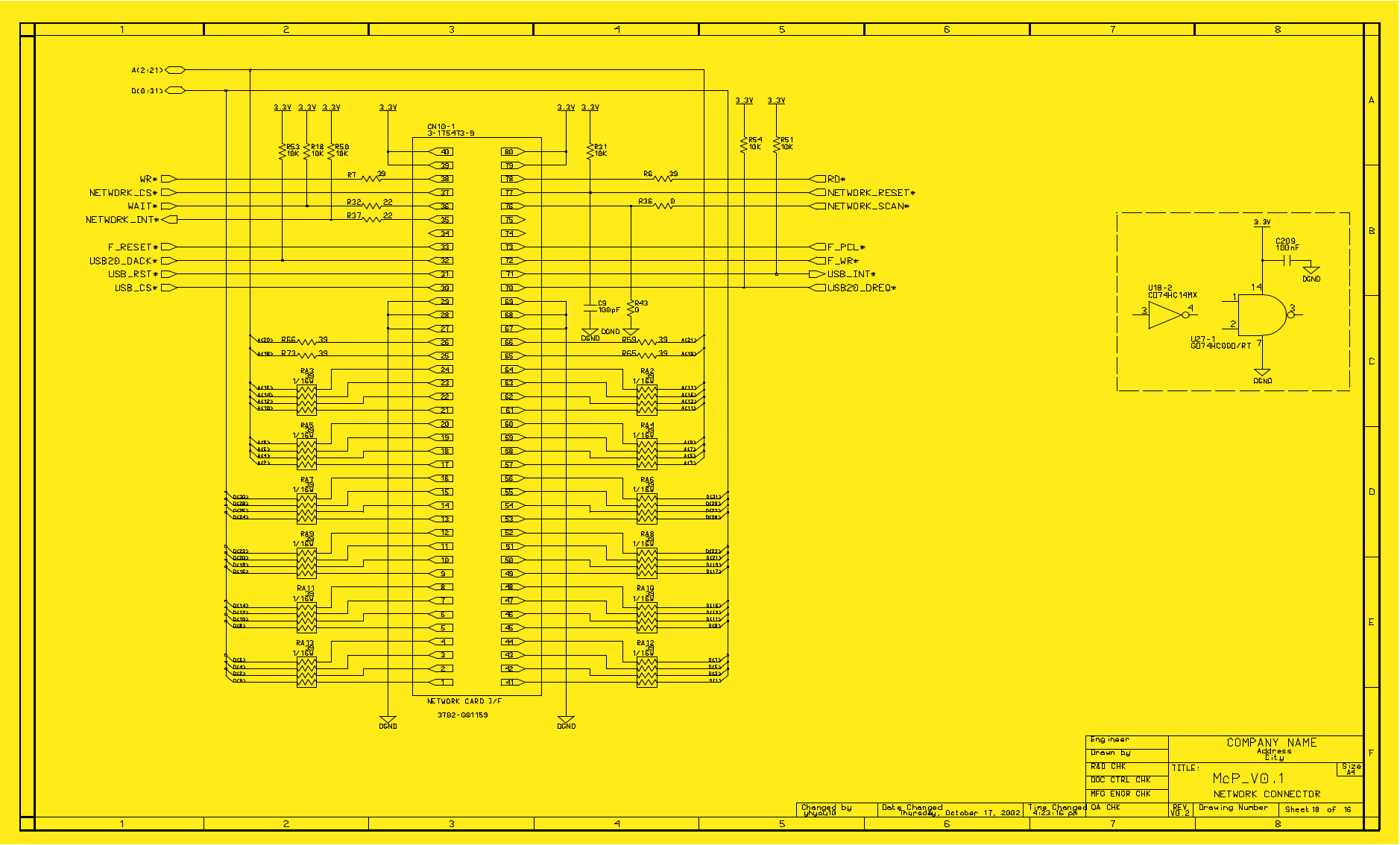
Main Circuit Diagram (8/16)



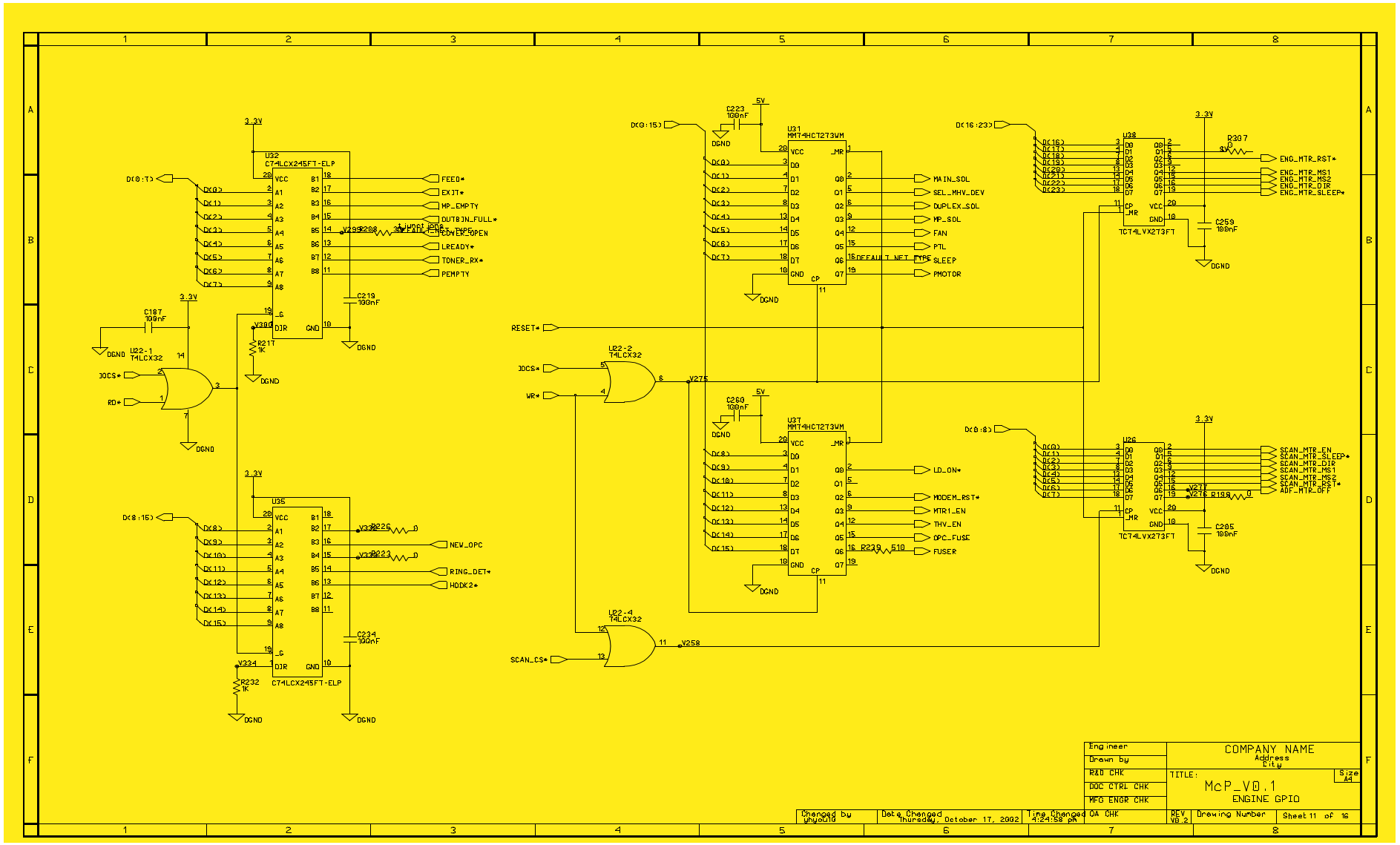
Main Circuit Diagram (9/16)



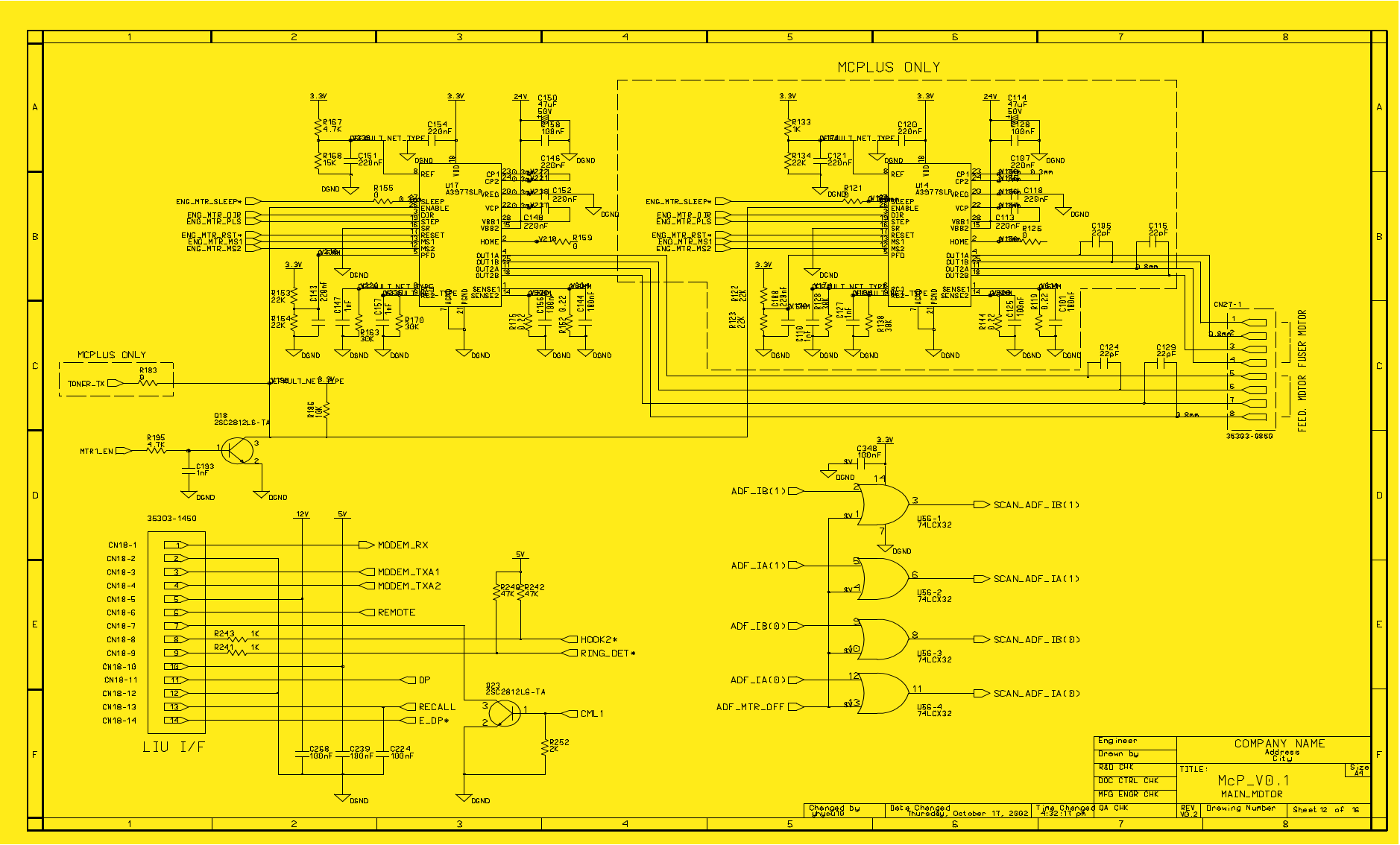
Main Circuit Diagram (10/16)



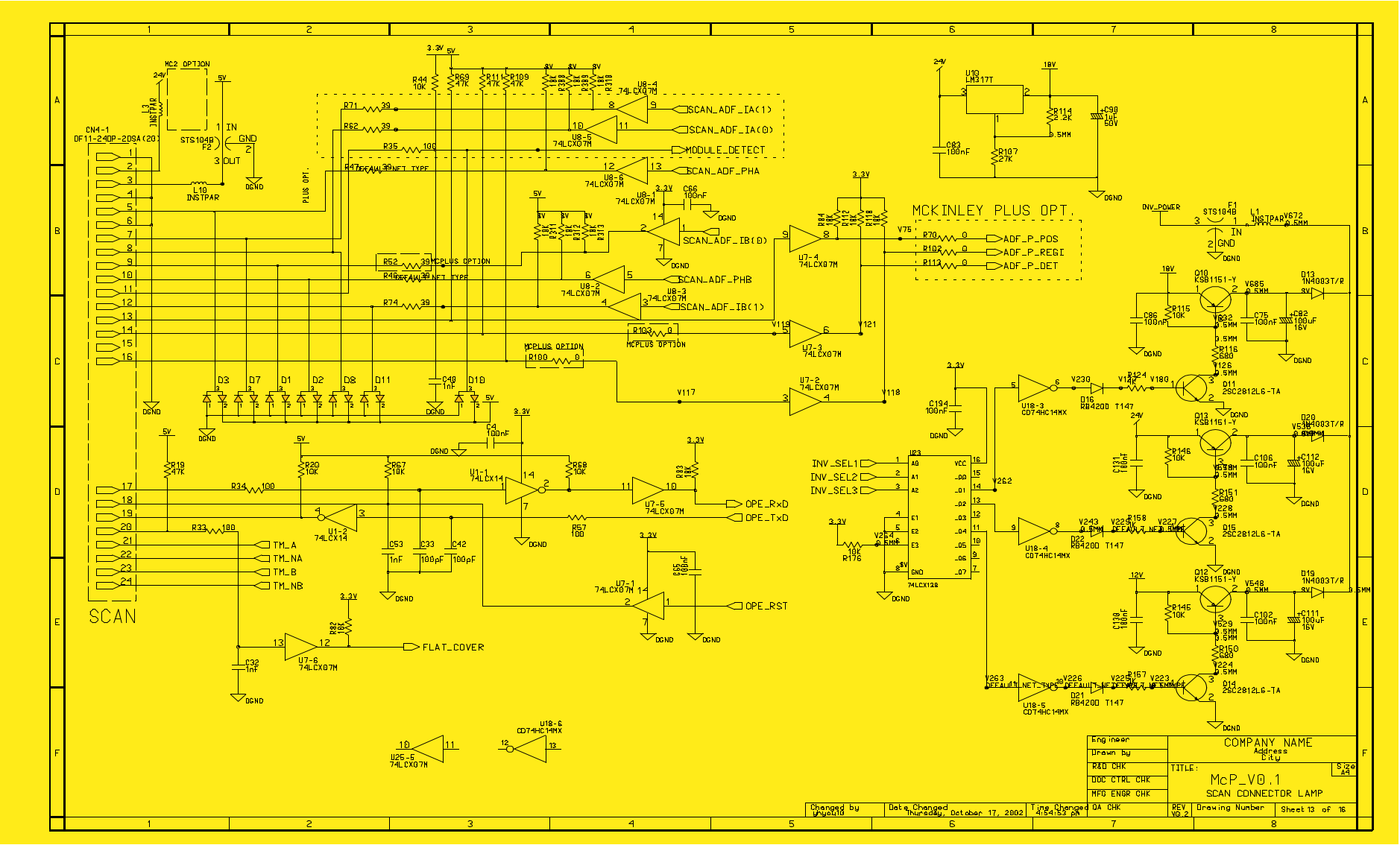
Main Circuit Diagram (11/16)



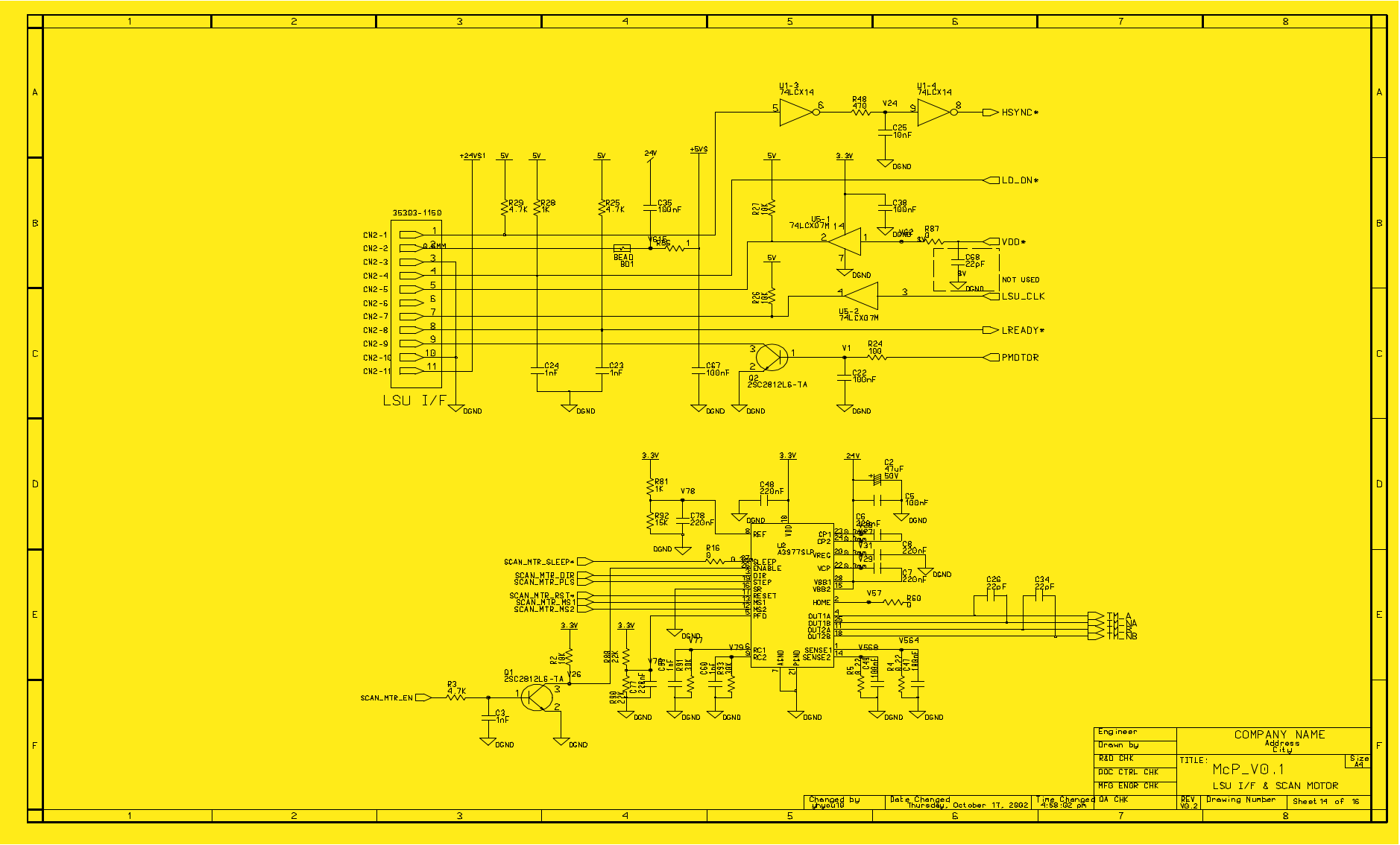
Main Circuit Diagram (12/16)



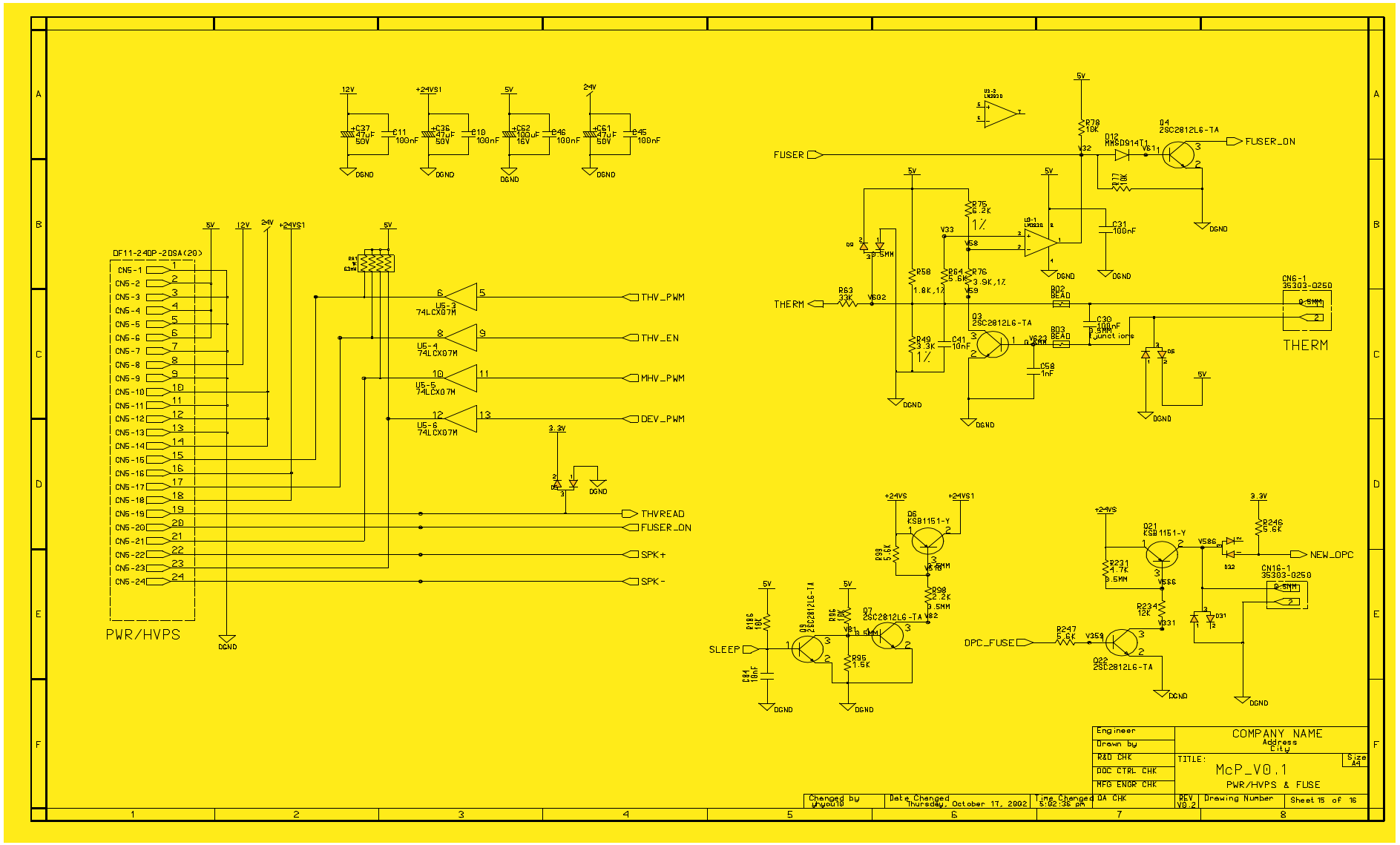
Main Circuit Diagram (13/16)



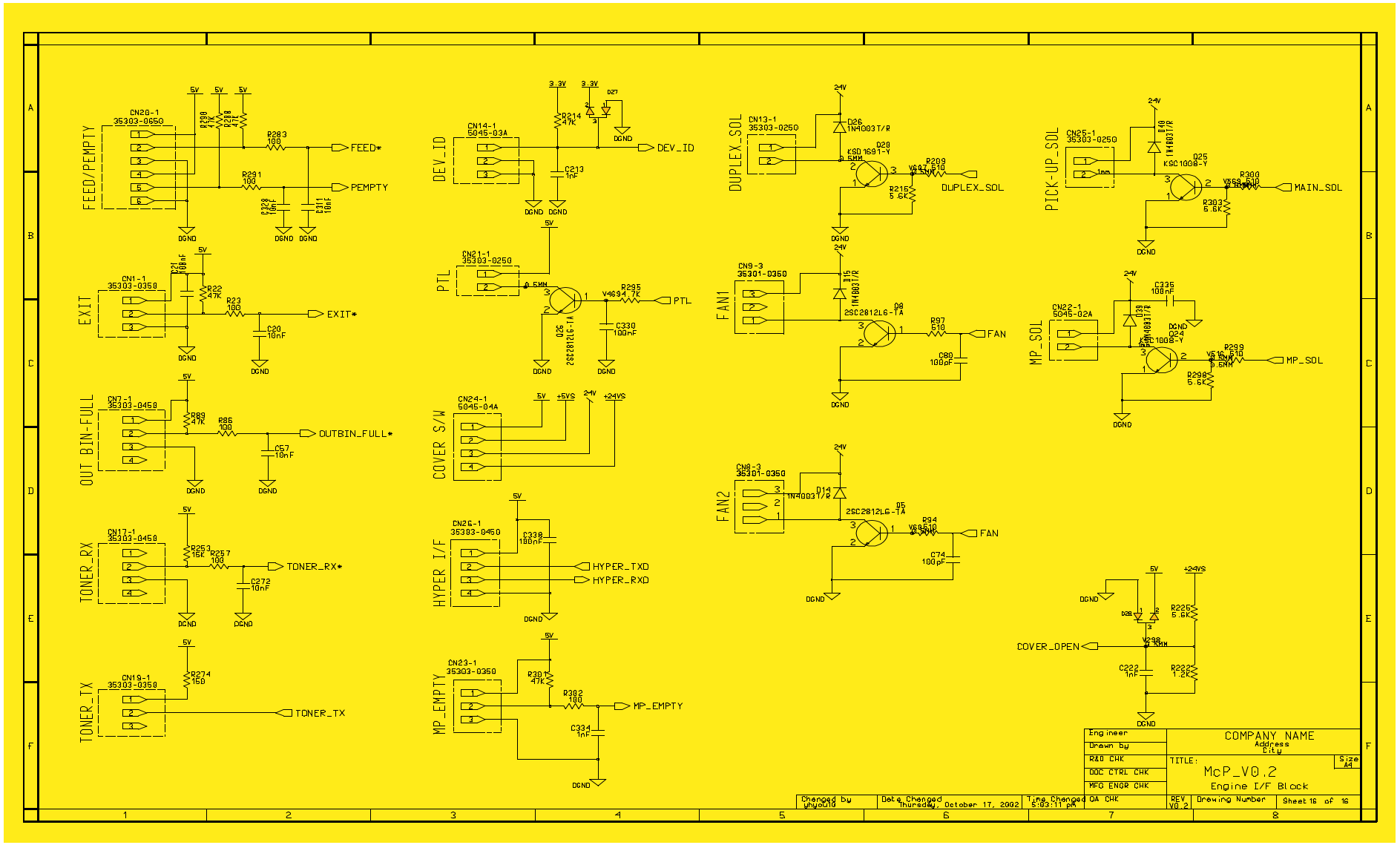
Main Circuit Diagram (14/16)



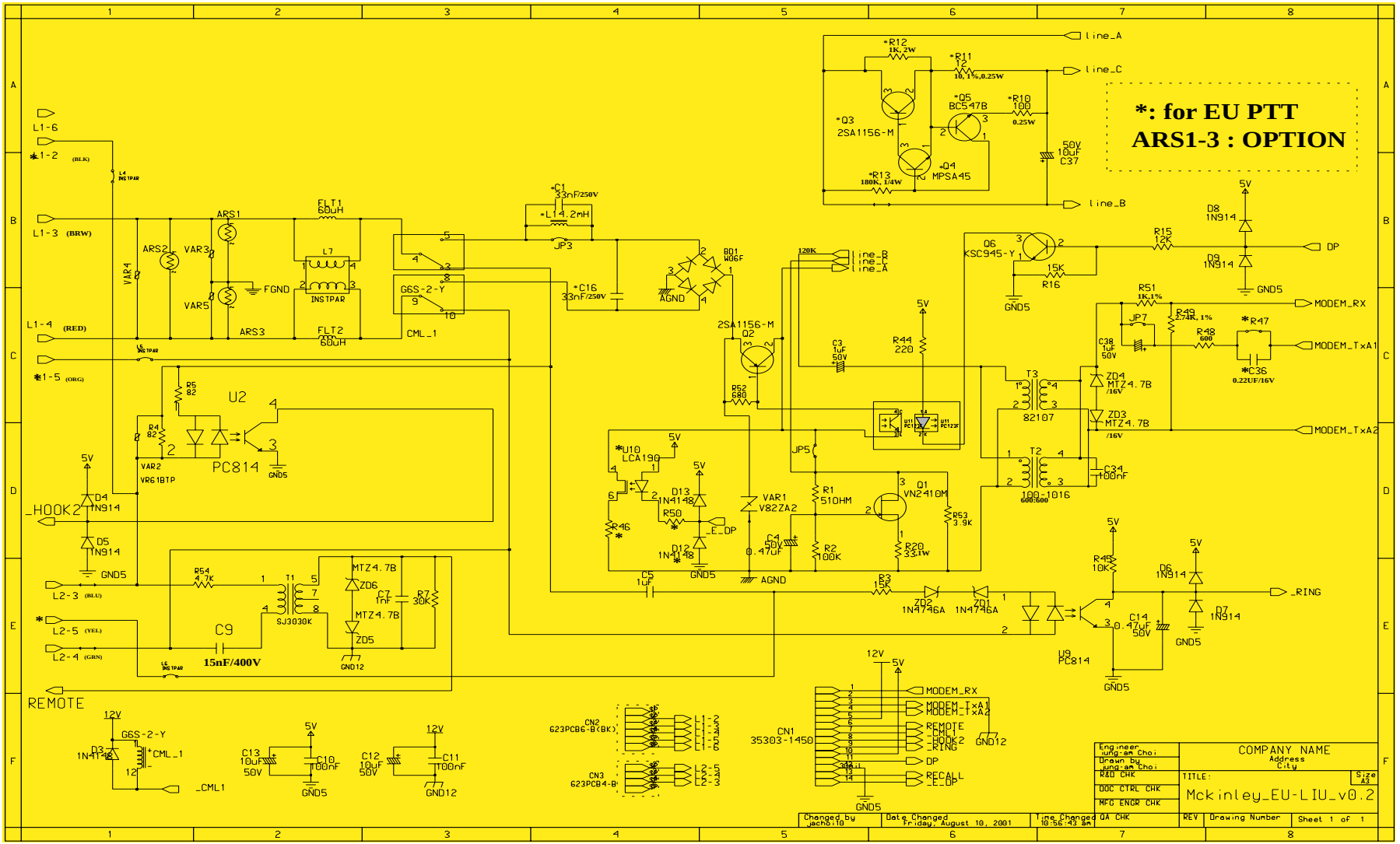
Main Circuit Diagram (15/16)



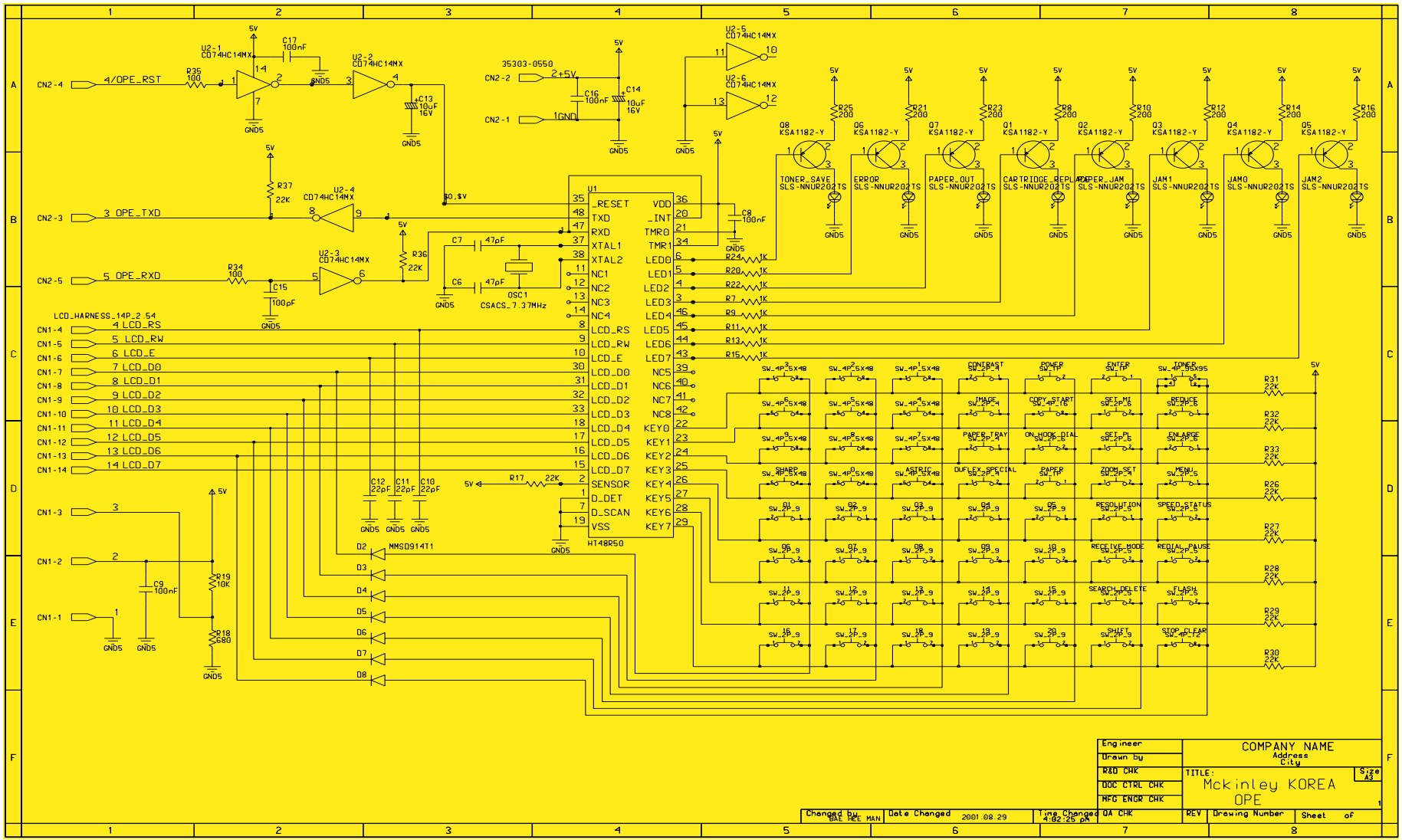
Main Circuit Diagram (16/16)



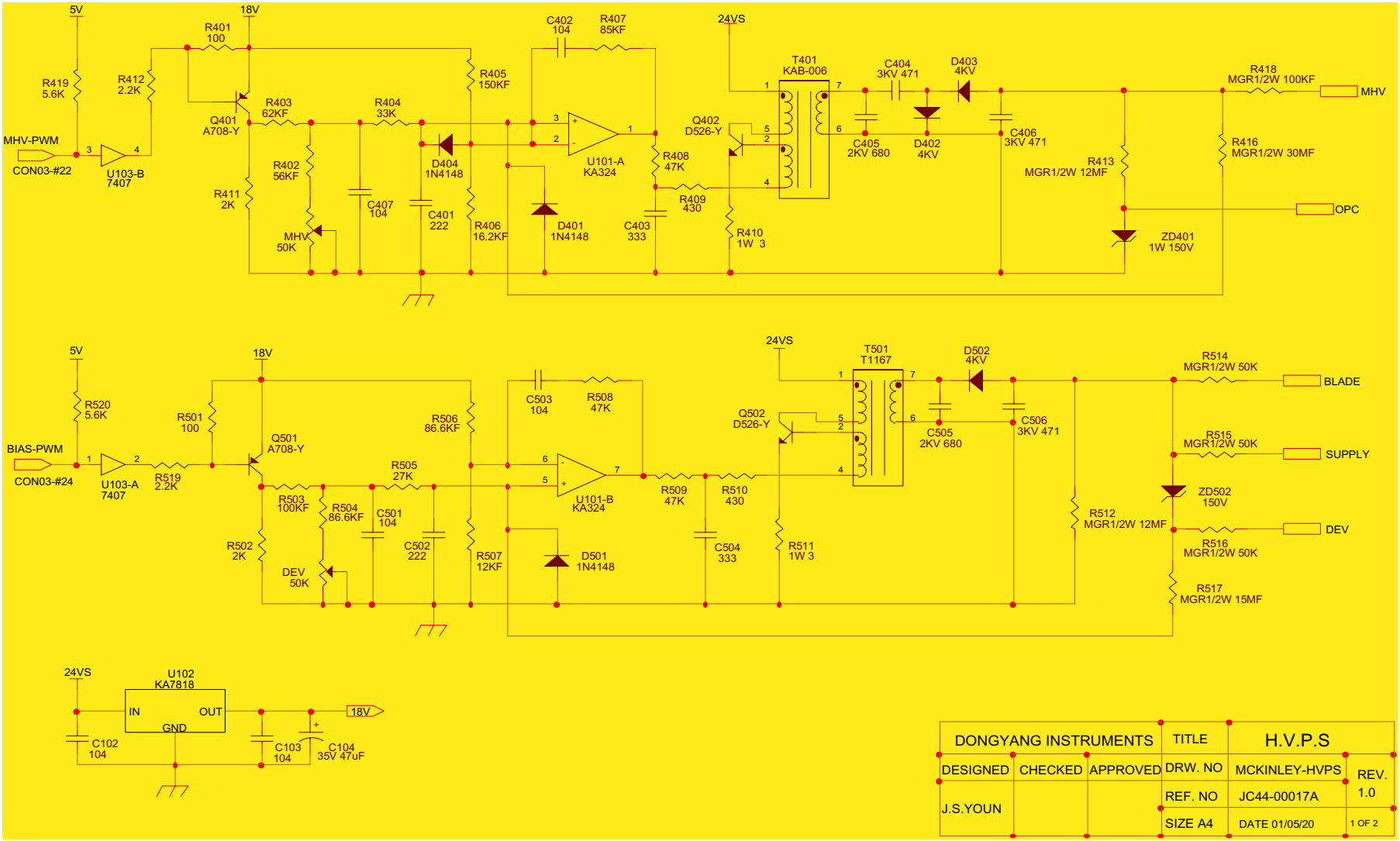
4-2 LIU Circuit Diagram



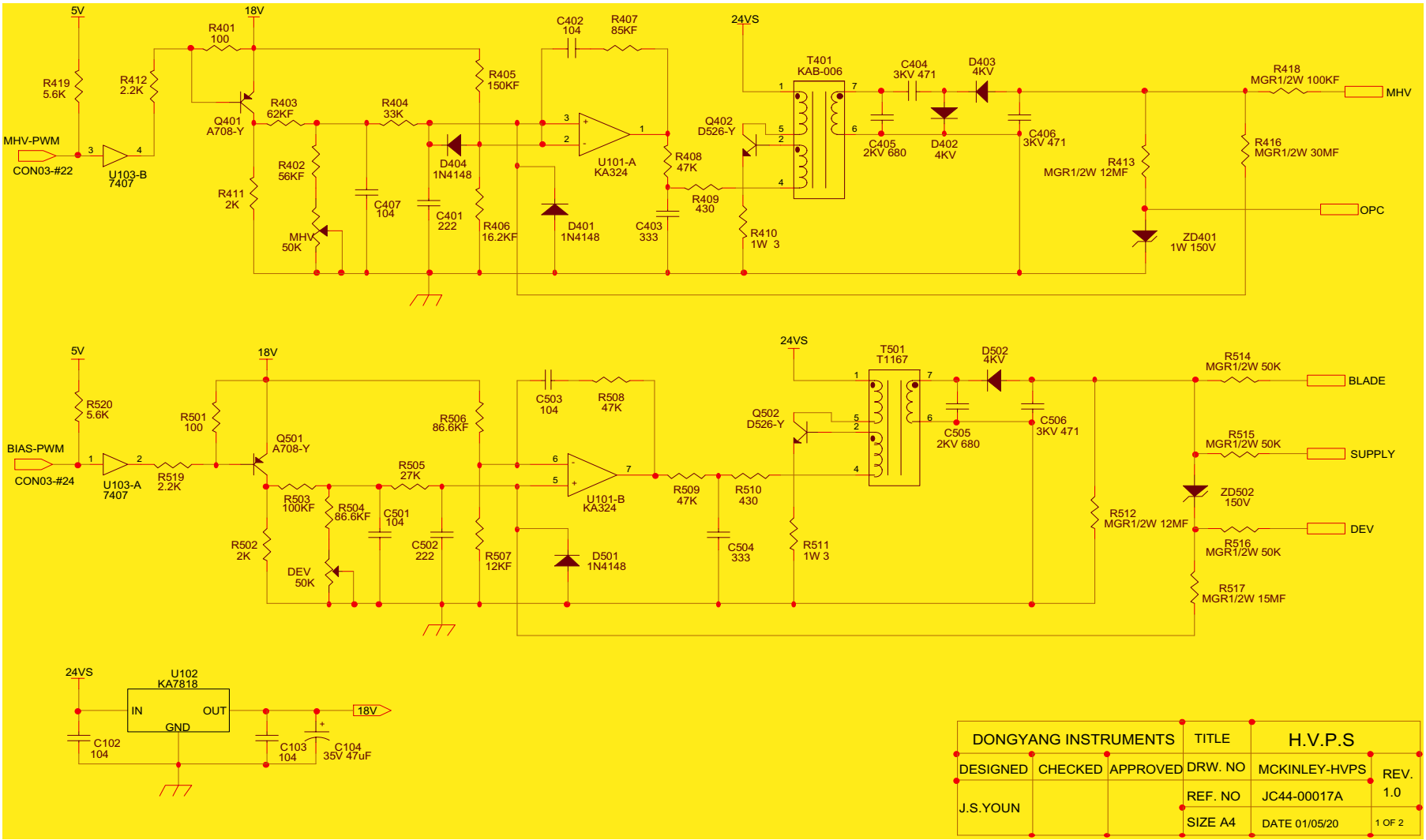
4-3 OPE Circuit Diagram



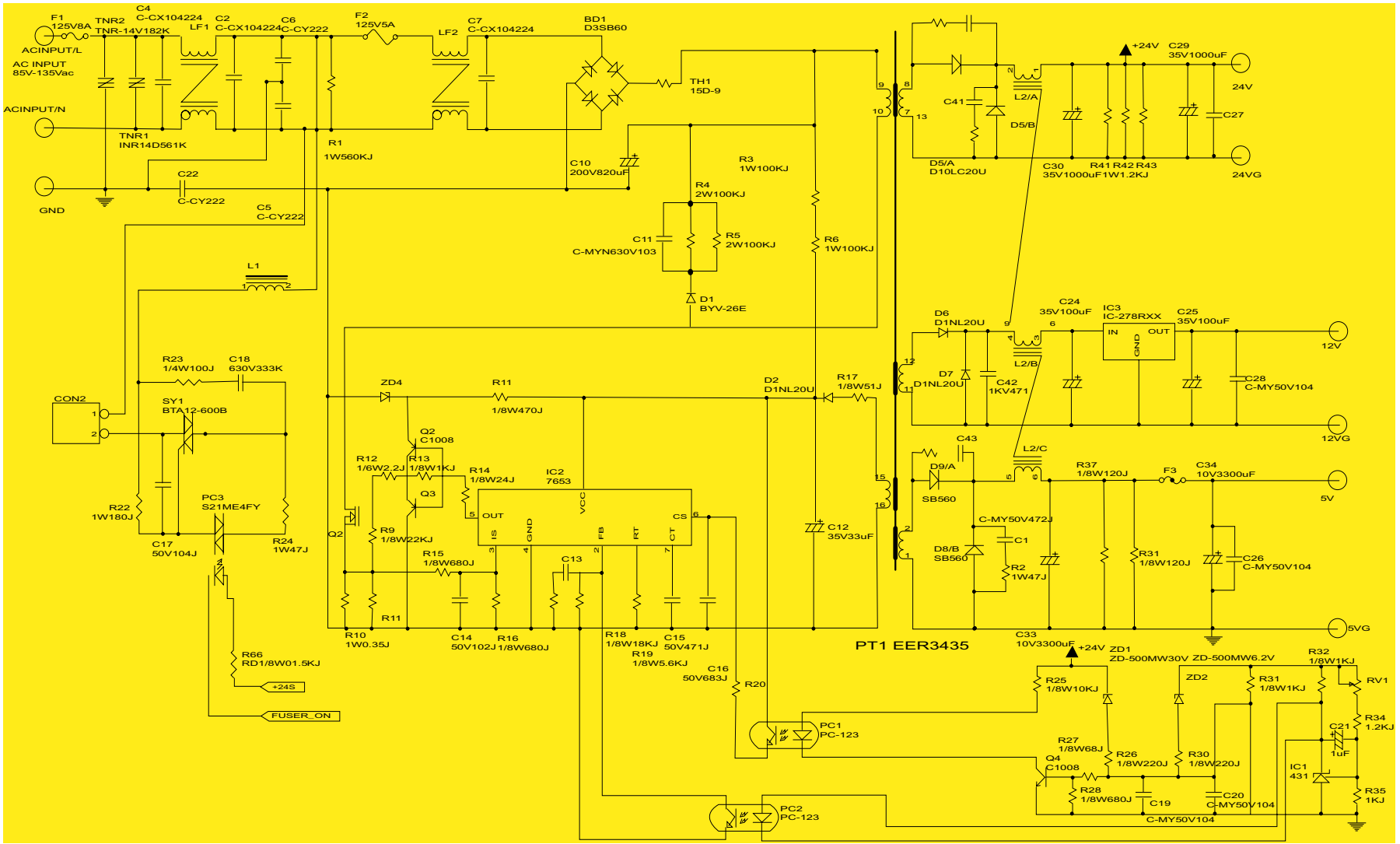
4-4 HVPS Circuit Diagram (1/2)



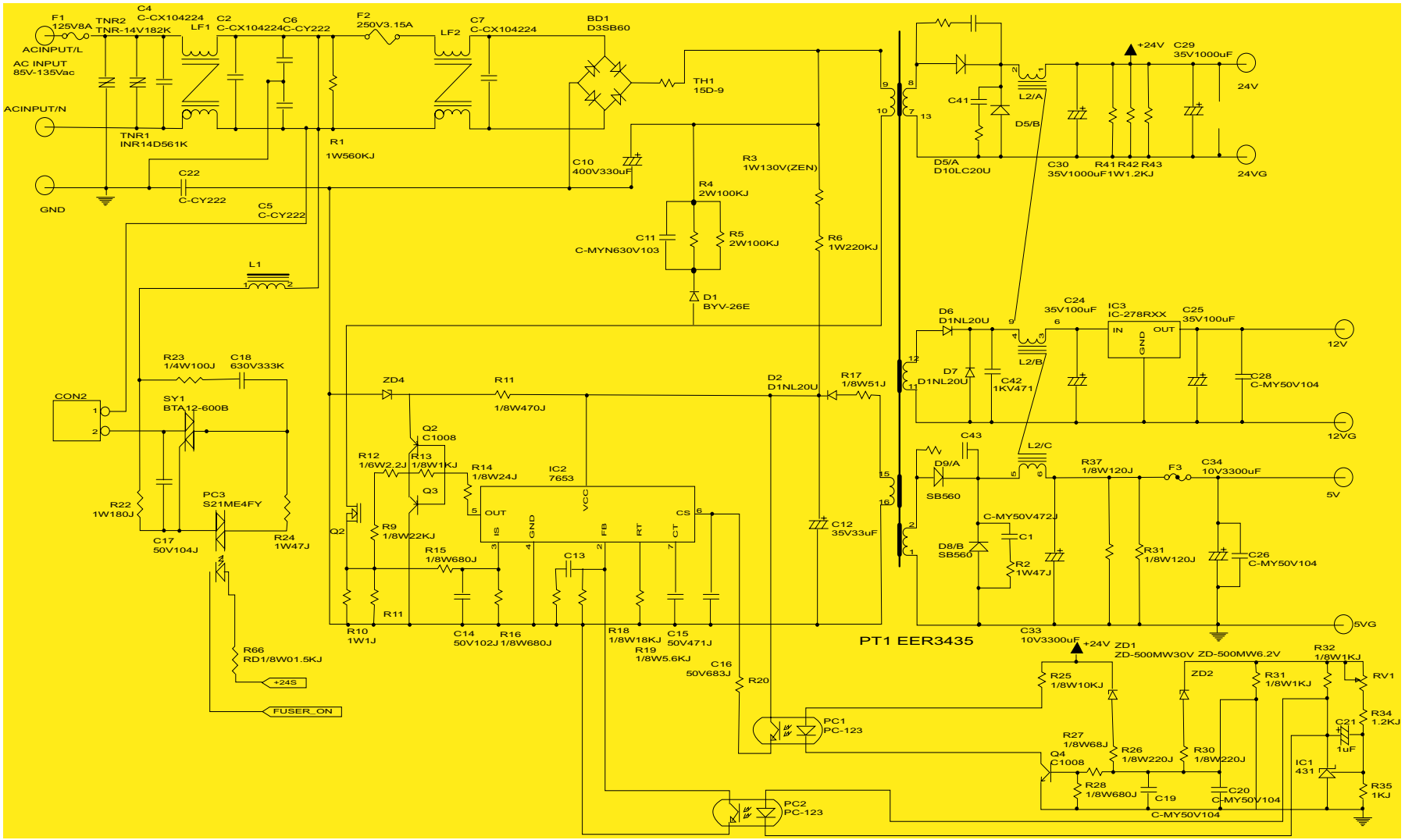
HVPS Circuit Diagram (2/2)



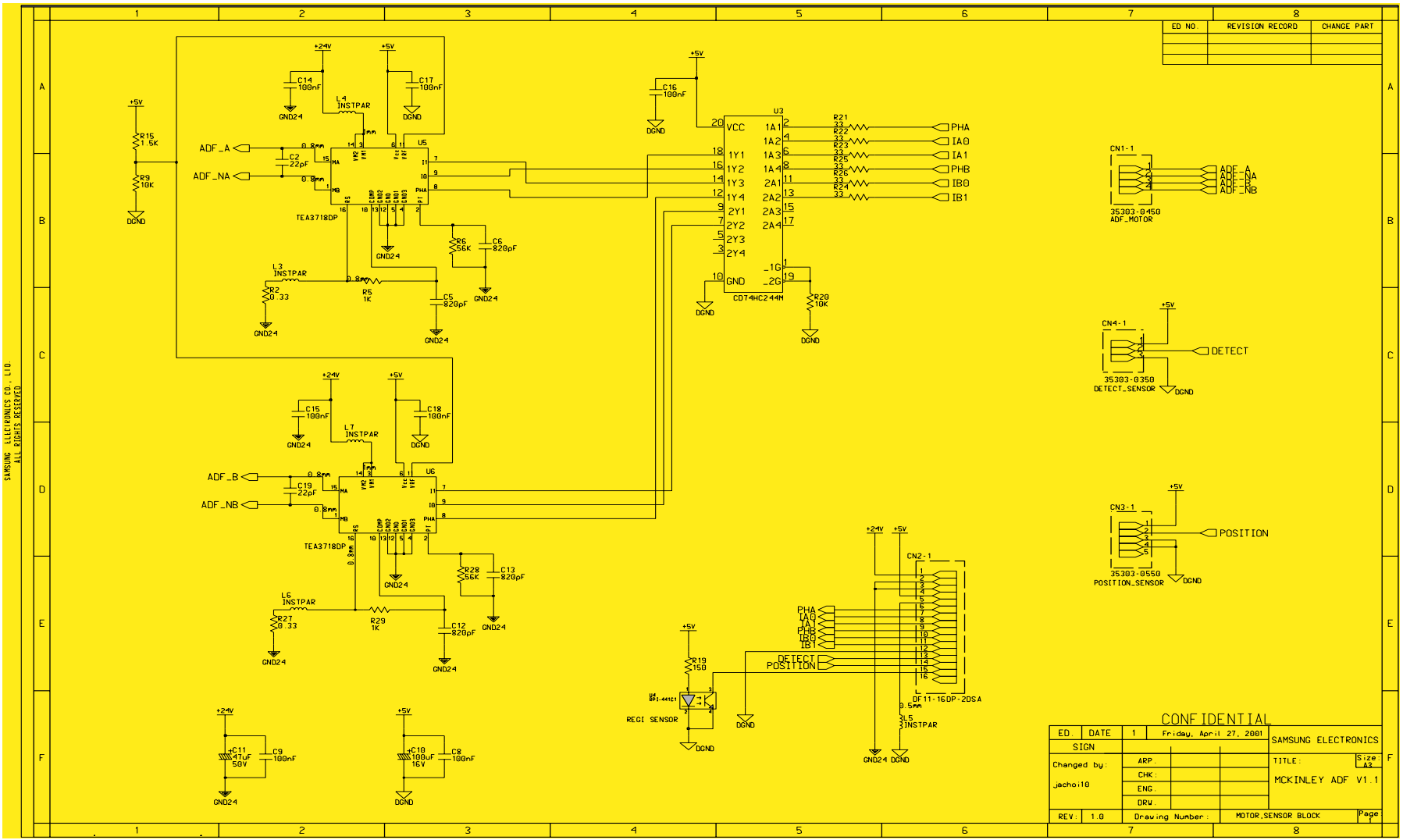
4-5 SMPS Circuit Diagram (110V)



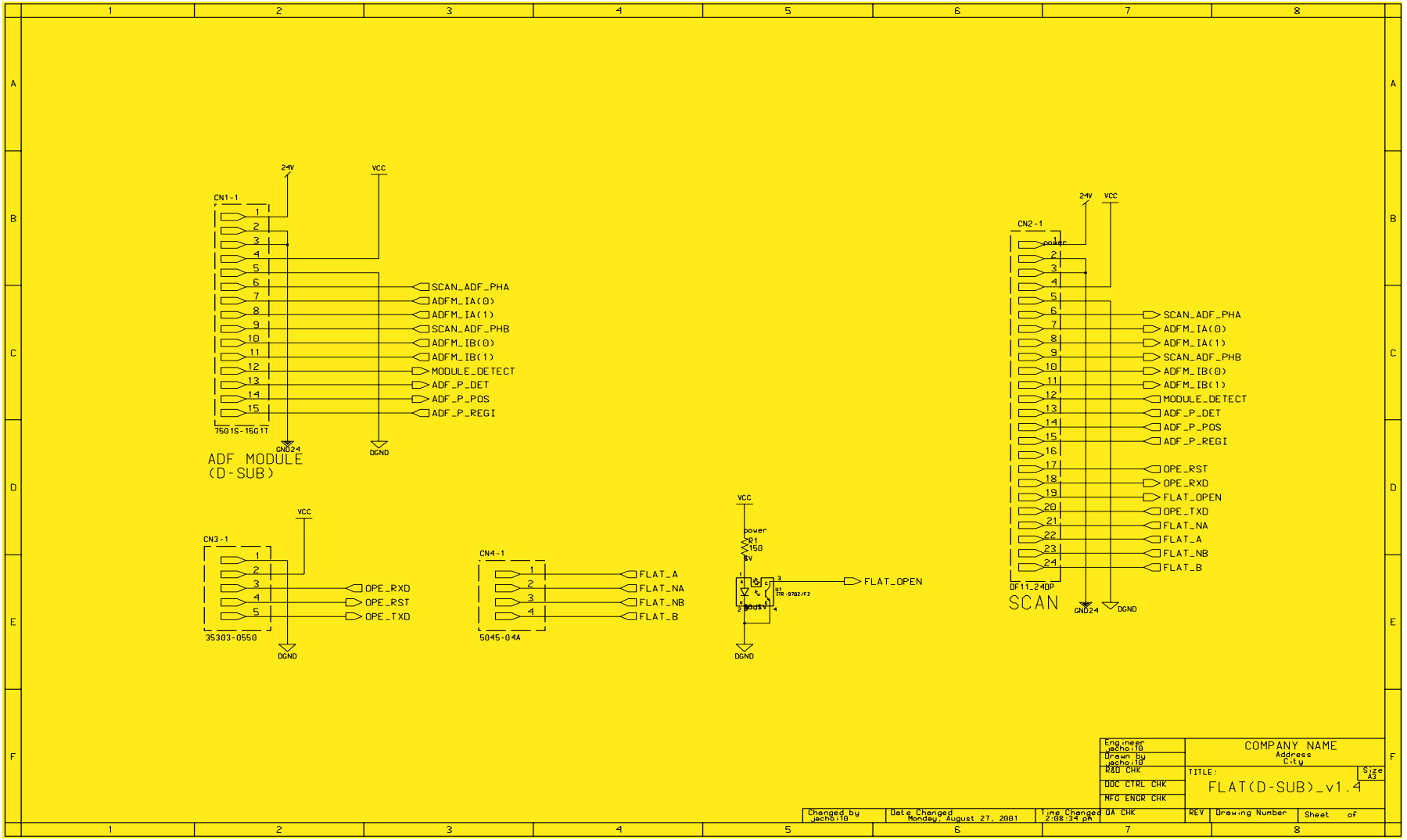
SMPS Circuit Diagram (220V)



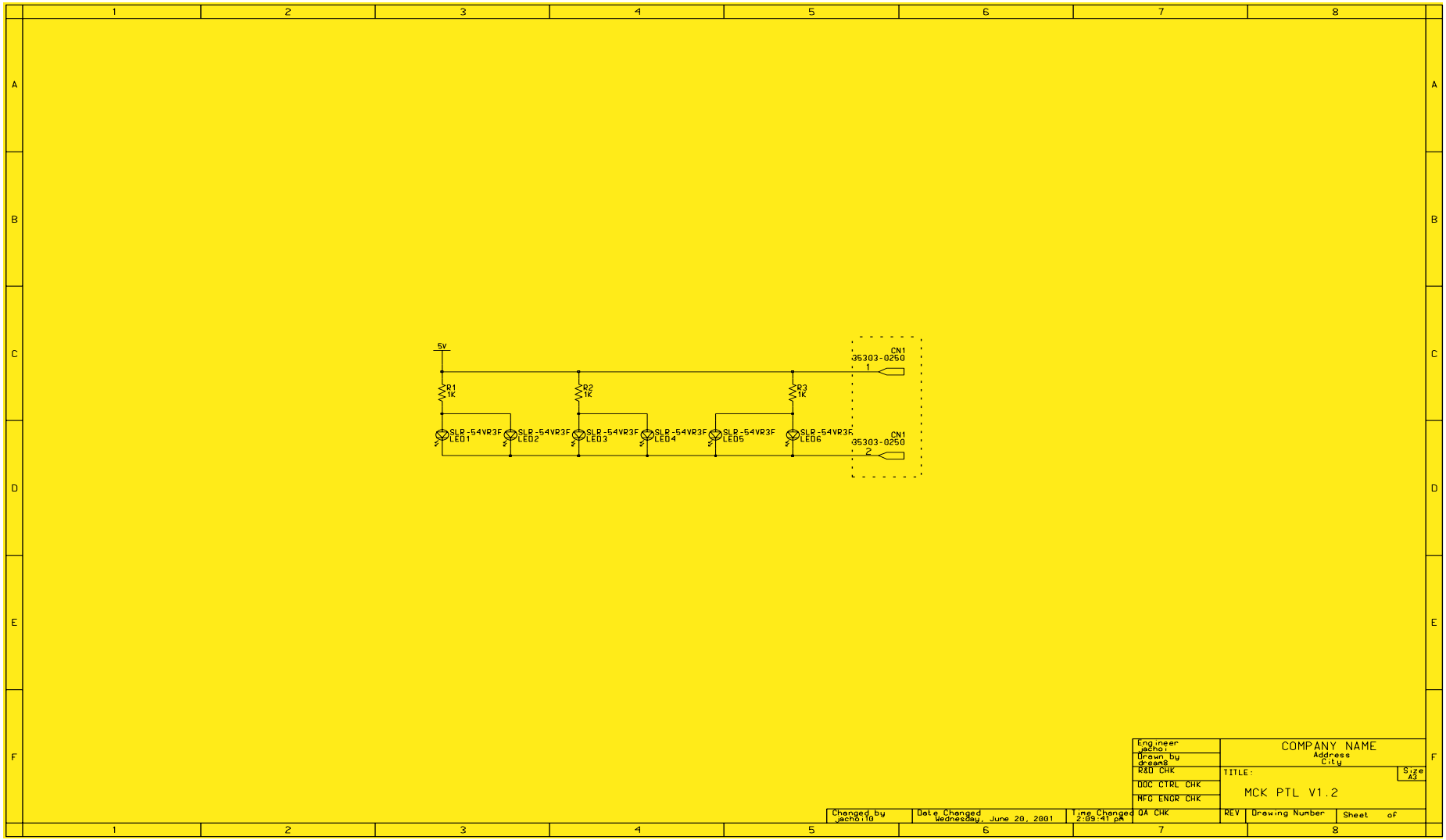
4-6 ADF Circuit Diagram



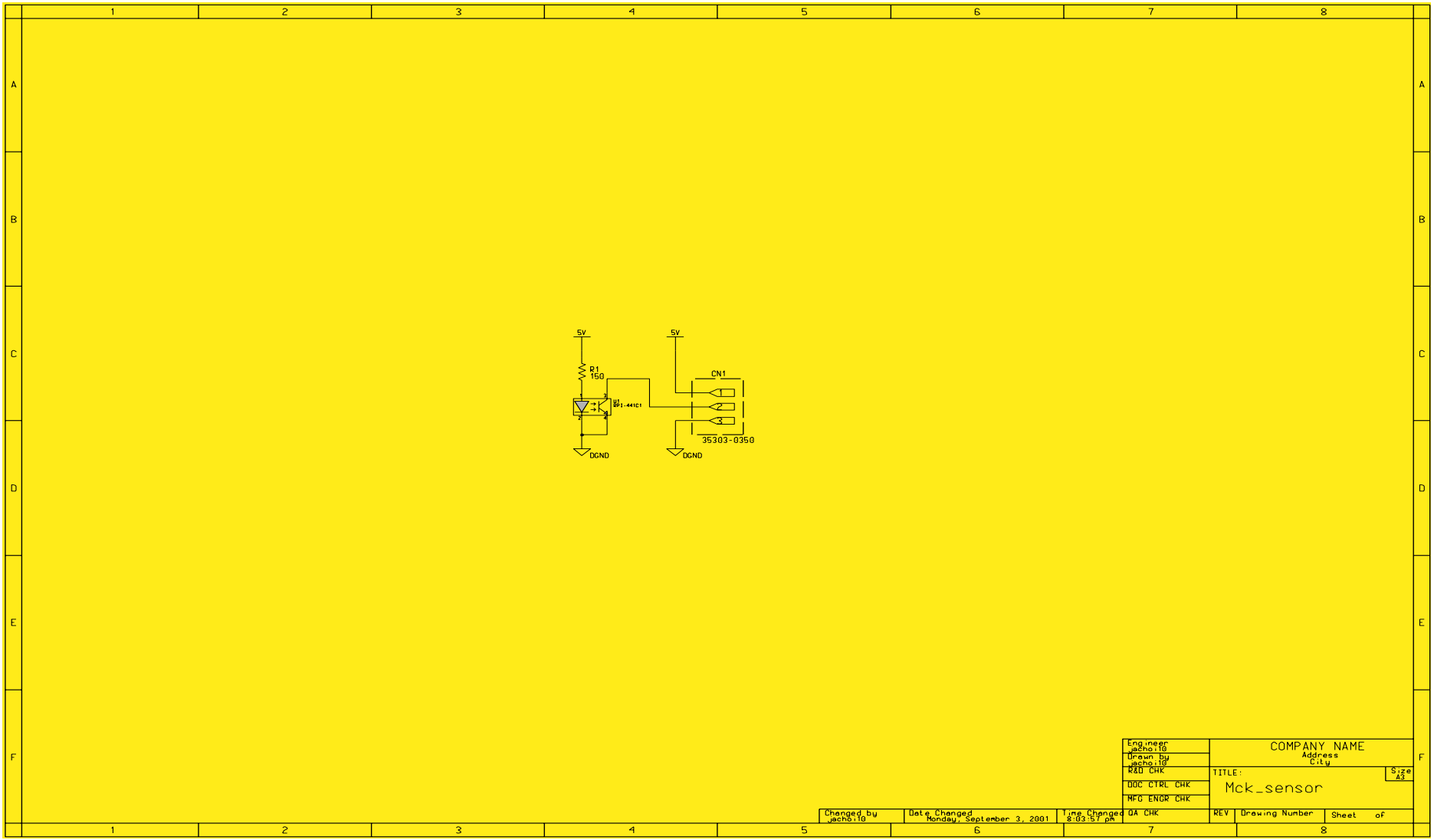
4-7 Flat Circuit Diagram



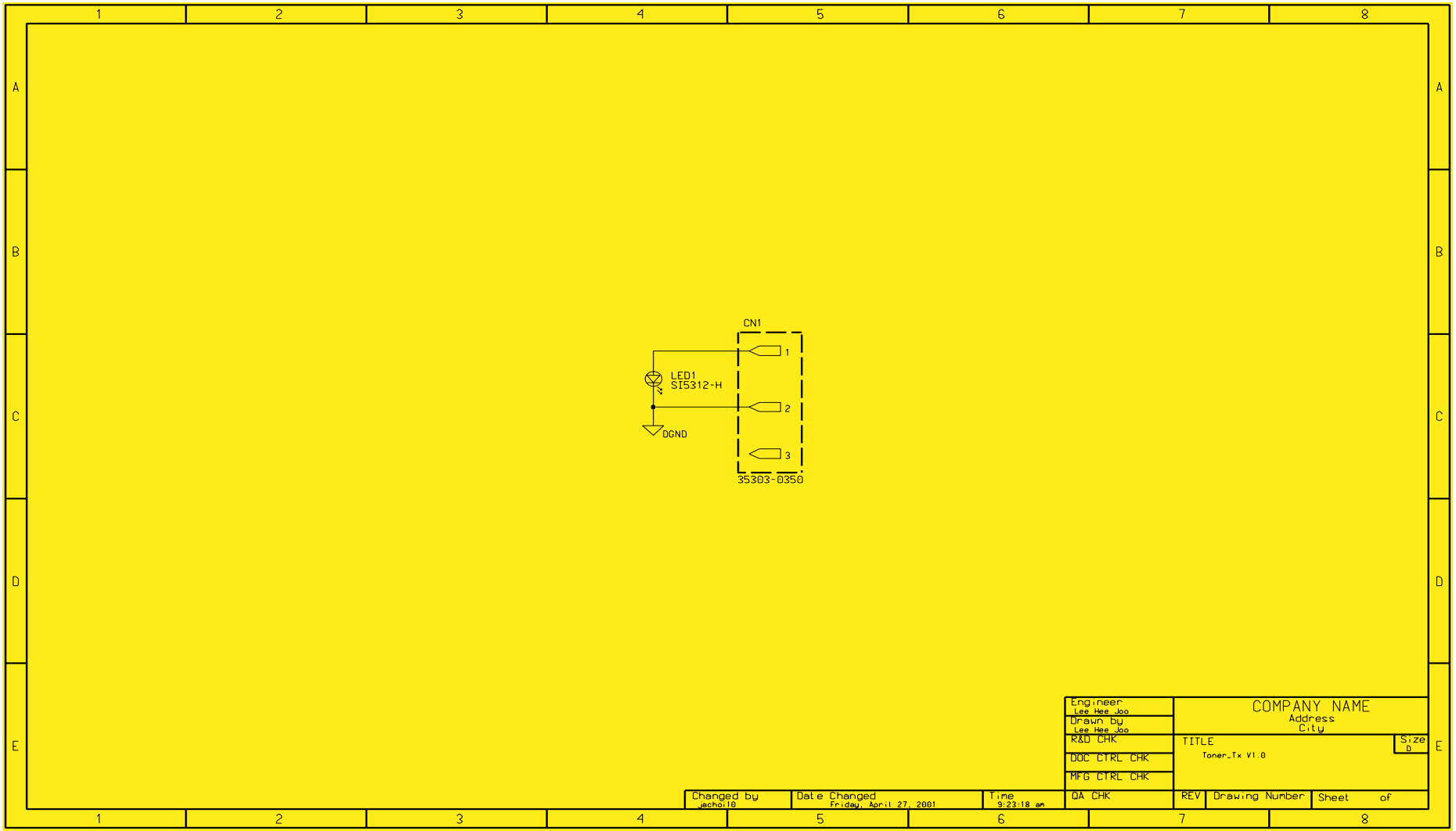
4-8 PTL Circuit Diagram



4-9 Sensor Circuit Diagram



4-10 Toner_Rx Circuit Diagram



4-11 Toner_Tx Circuit Diagram